



IC780M-A2

V :1.0A

SCHEMATICS TABLE:

Page	Index
1	COVER PAGE
2	BLOCK DIADRAM
3	AM3 CPU HT & OVERCLOCK
4	AM3 CPU MEMORY
5	AM3 CPU CONTROL & MISC
6	AM3 CPU PWR & GND
7	DDR3 DIMM A CHANNEL
8	DDR3 DIMM B CHANNEL
9	DDR3 DIMM POWER
10	CLOCK GEN ICS9LPRS471
11	CPU VCORE ISL6323
12	NB POWER
13	DC-DC
14	FRONT PANEL/FAN PNL
15	RX780 HT LINK I/F
16	RX780 PCIE I/F&STRAPS
17	RX780 SYSTEM I/F
18	RX780 POWER
19	PCI-E X16 CONN

REVISION HISTORY:

Rev	Date	Notes
A	2009/07	INITIAL RELEASE
1.0	2009/09	add ACC fuction,Fixed A3 issue

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IMPORTANT NOTES ABOUT THIS SCHEMATIC

- DESIGN NOTE: Example text for the design note to show the note inside the colored box.

1) DESIGN NOTES in grey are information notes.
- DESIGN NOTE: Example text for the design note to show the note inside the colored box.

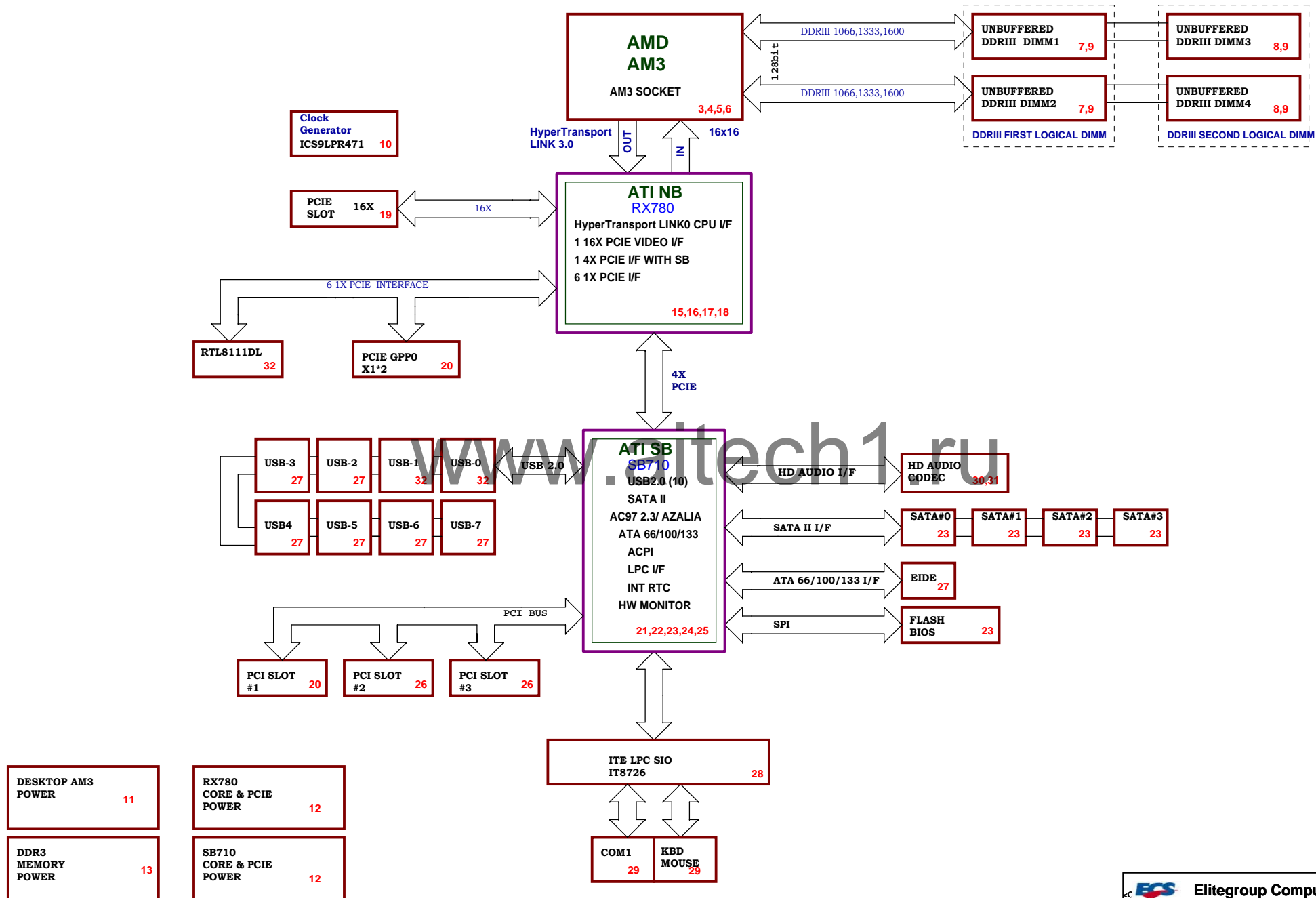
2) DESIGN NOTES in yellow are notes of caution.
- DESIGN NOTE: Example text for the design note to show the note inside the colored box.

3) DESIGN NOTES in red are critical, and must be understood and followed.

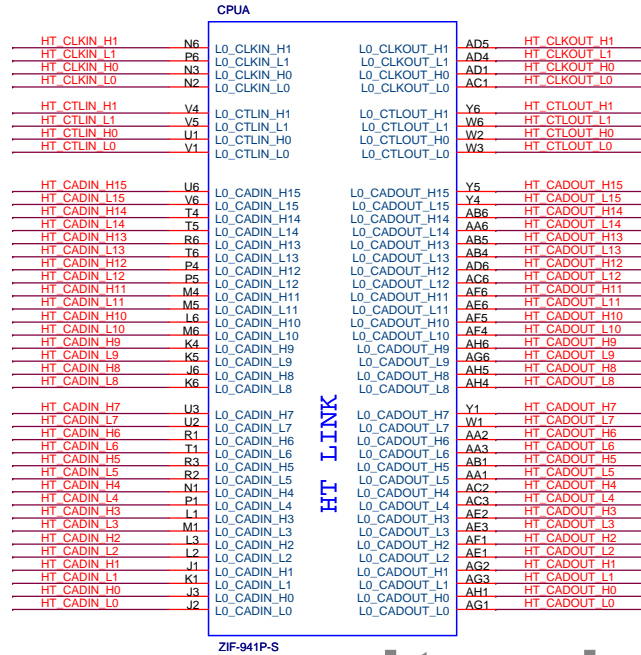
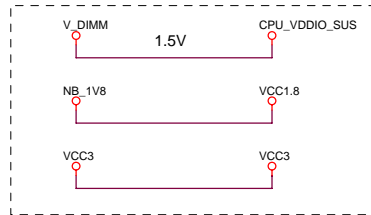
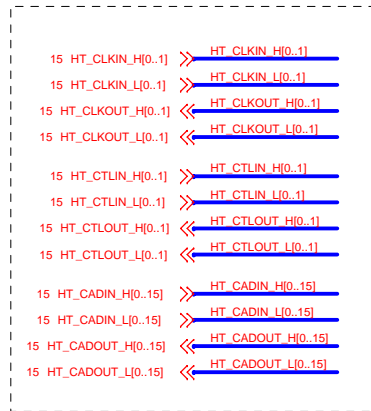
@ ECS CONFIDENTIAL @

PCB STACK: L1:TOP
L2:PWR
L3:GND
L4:BOTTOM

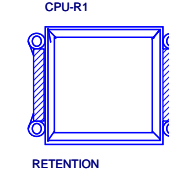
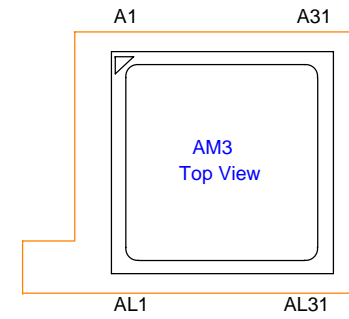
Elitegroup Computer Systems			
Title			
Cover Page			
Size	Document Number	Rev	
Custom	IC780M-A2	1.0A	
Date:	Thursday, October 15, 2009	Sheet	1 of 36



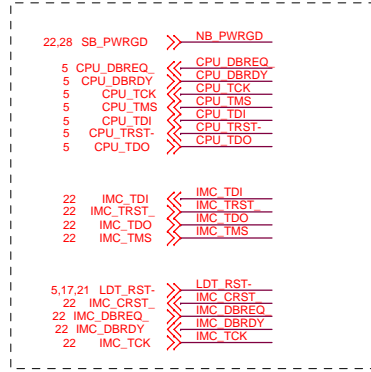
HyperTransport



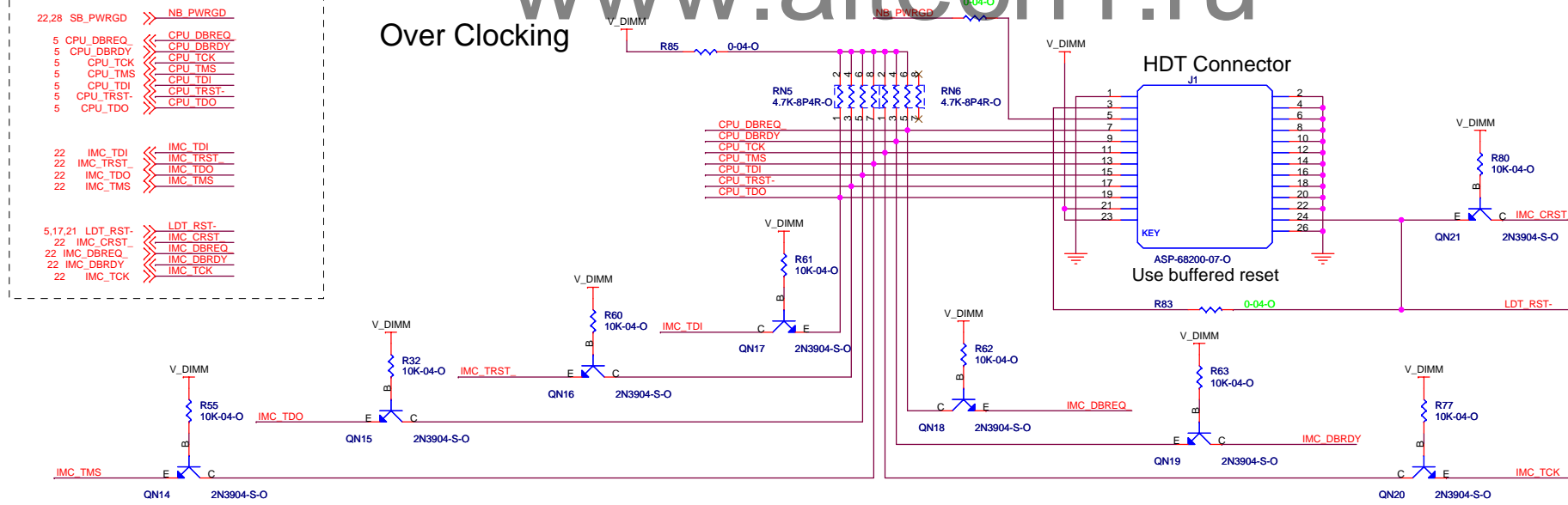
Please use 1mm pad size,
place all ELT test pads
on bottom side only.



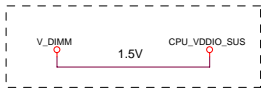
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Over Clocking

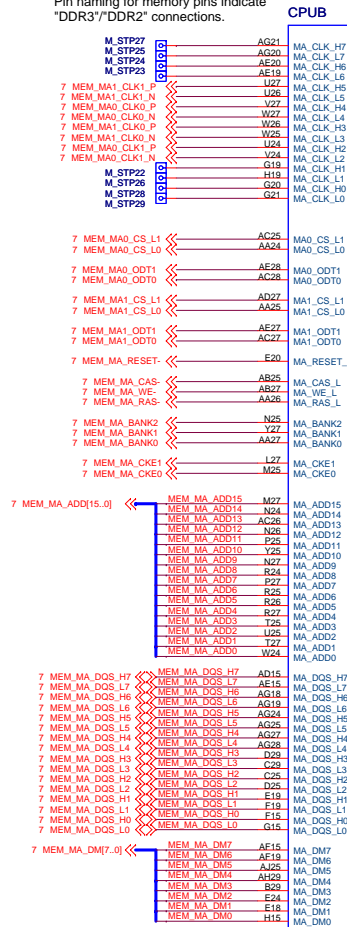


CPU Memory



DDR3 Memory Interface A

Pin naming for memory pins indicate
"DDR3"/"DDR2" connections.



ZIF-941P-S

MEMORY CLOCK TRANSLATION

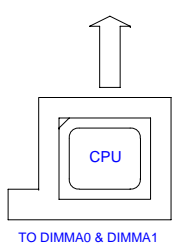
DIMM	DDR3 Memory Signal	CPU Signal
DIMM A0	MEM_MA0_CLKL1	MA_CLK2
	MEM_MA0_CLKL0	MA_CLK4
DIMM A1	MEM_MA1_CLKL1	MA_CLK5
	MEM_MA1_CLKL0	MA_CLK3
DIMM B0	MEM_MB0_CLKL1	MB_CLK2
	MEM_MB0_CLKL0	MB_CLK4
DIMM B1	MEM_MB1_CLKL1	MB_CLK5
	MEM_MB1_CLKL0	MB_CLK3

DDR3 Memory Interface B

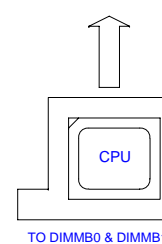
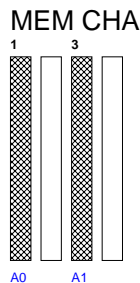
Pin naming for memory pins indicate
"DDR3"/"DDR2" connections.



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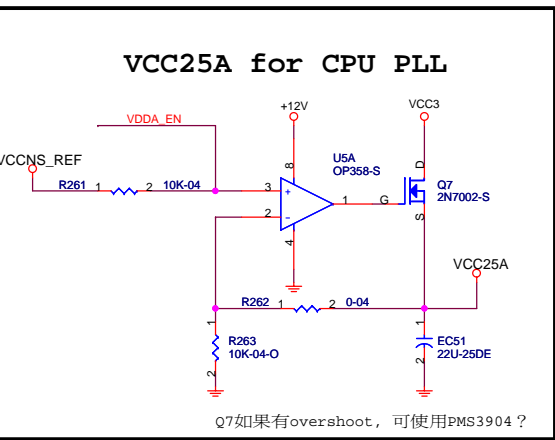
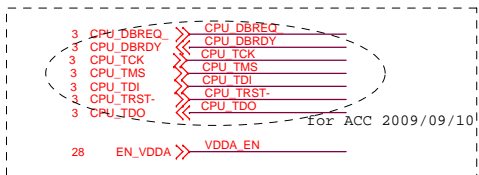
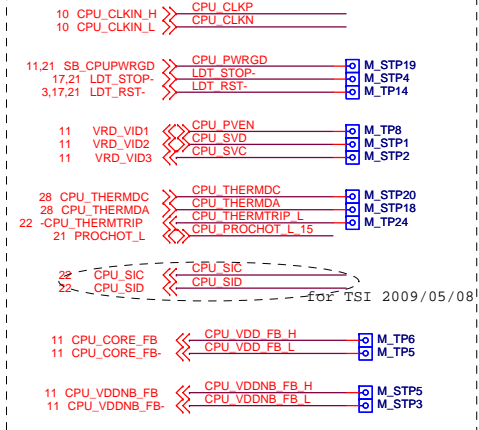
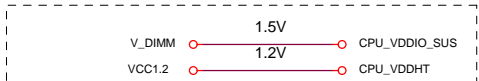
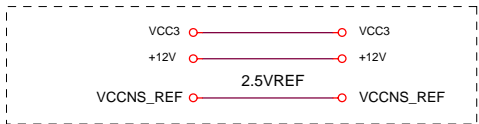
TO DIMMA0 & DIMMA1



TO DIMMB0 & DIMMB1

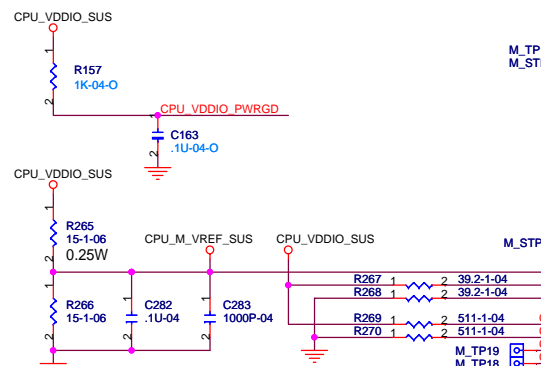


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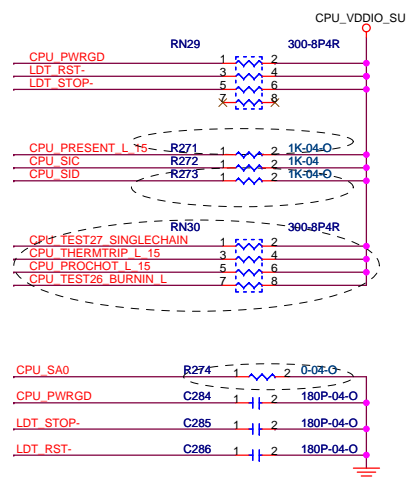
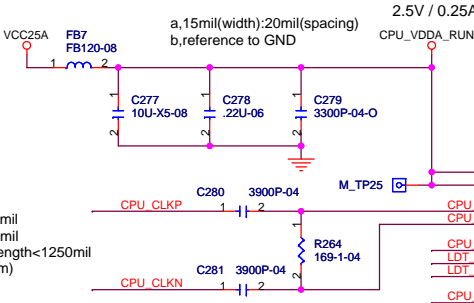


Q7如果有overshoot, 可使用PMS3904?

a, Rshunt near CPU pin<600mil
b, Cseries as a pair within 25mil
c, Cseries to CPU pin trace length<1250mil
d, 12:4:6:4:12(1080 for 930hm)

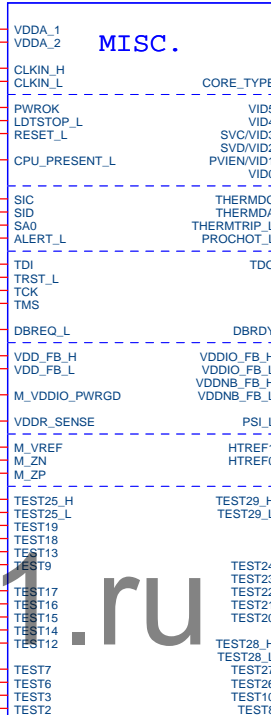


12mil(width):20mil(spacing)



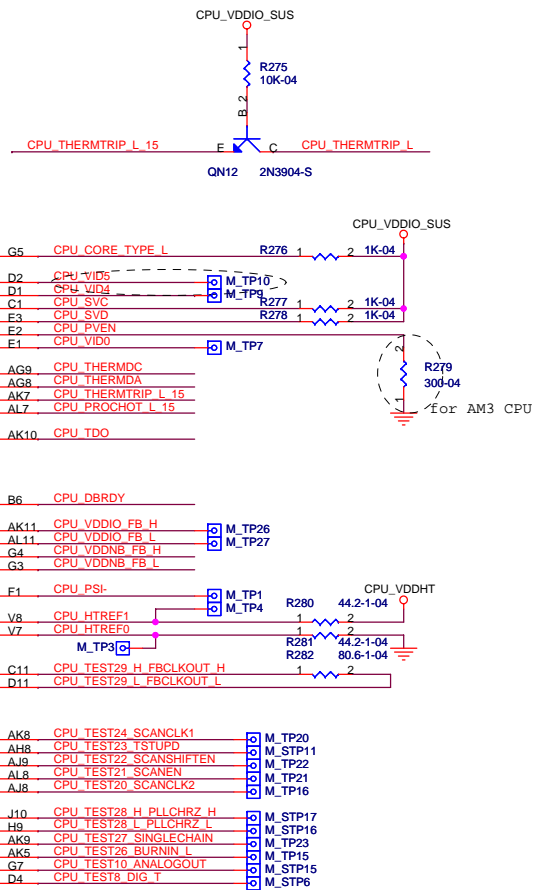
CPU

MISC.



INT. MISC.

ZIF-941P-S



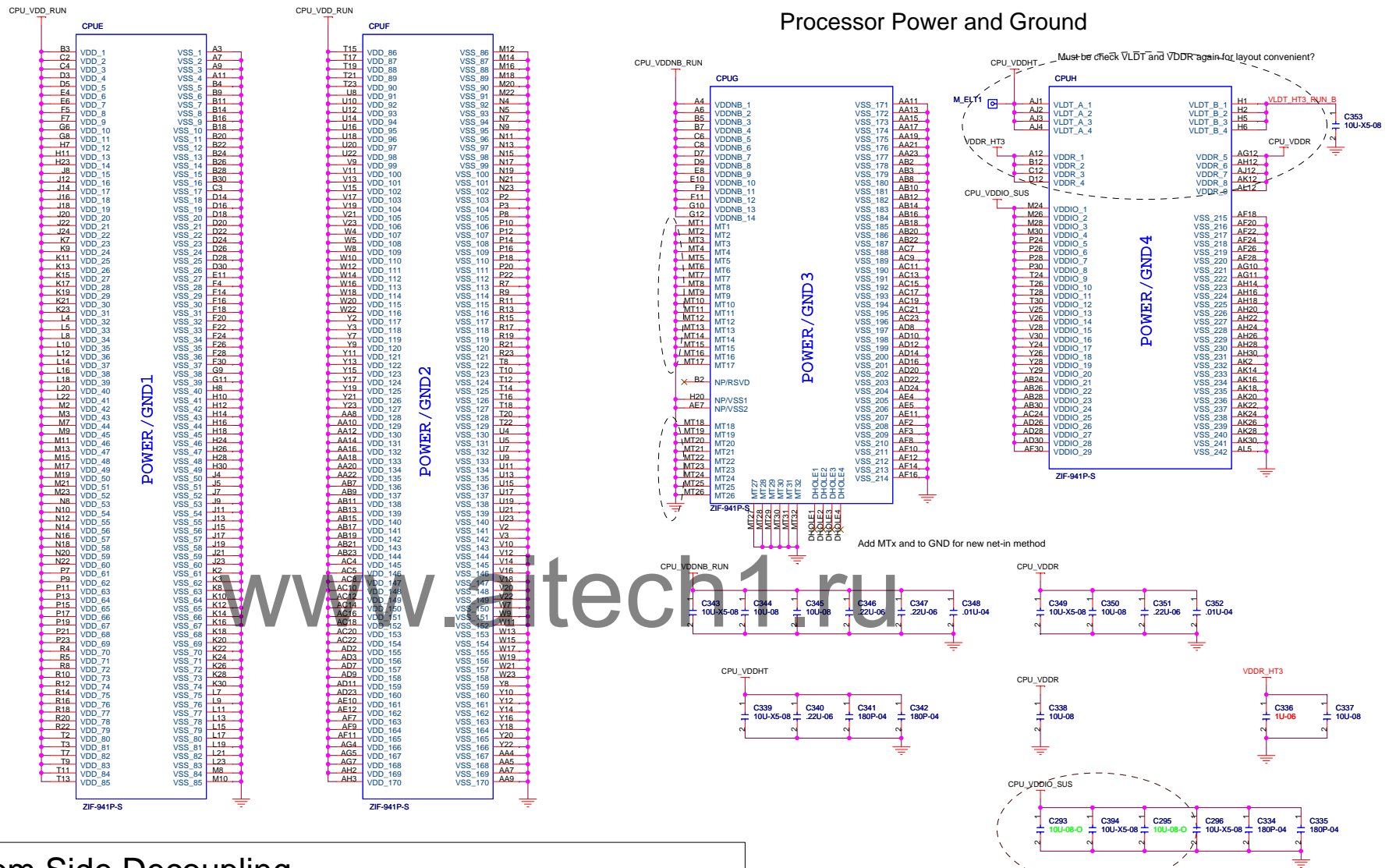
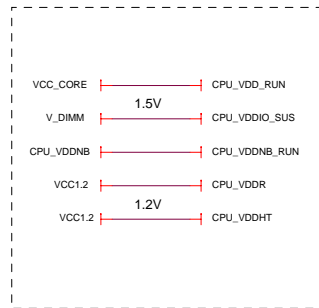
Layout: Route as 80 ohms diff impedance.
Keep trace to resistor < 1" from CPU pins.



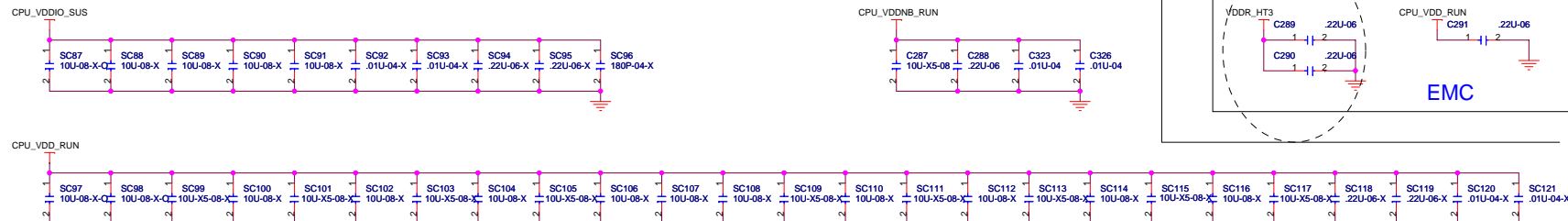
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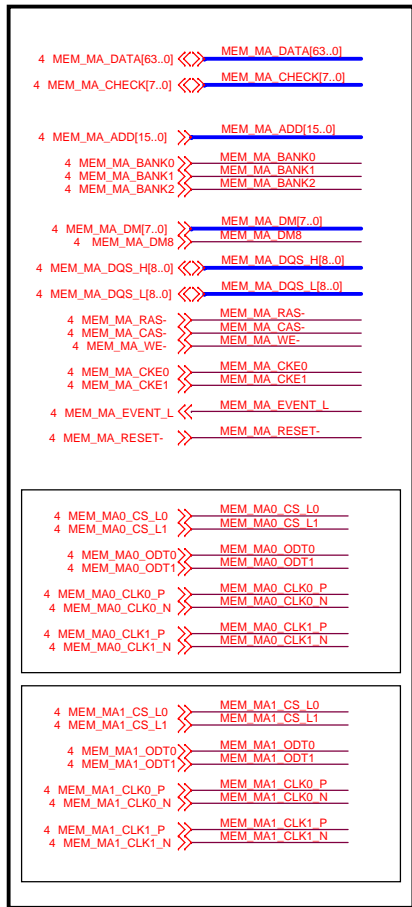
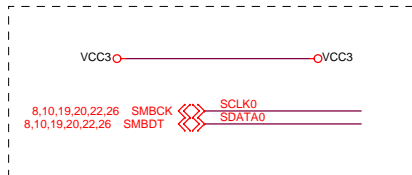
AM3 CPU CONTROL&MISC			
Rev	1.0A		
Size	Document Number	IC780M-A2	
Custom			
Date:	Thursday, October 15, 2009	Sheet	5 of 36

Processor Power and Ground

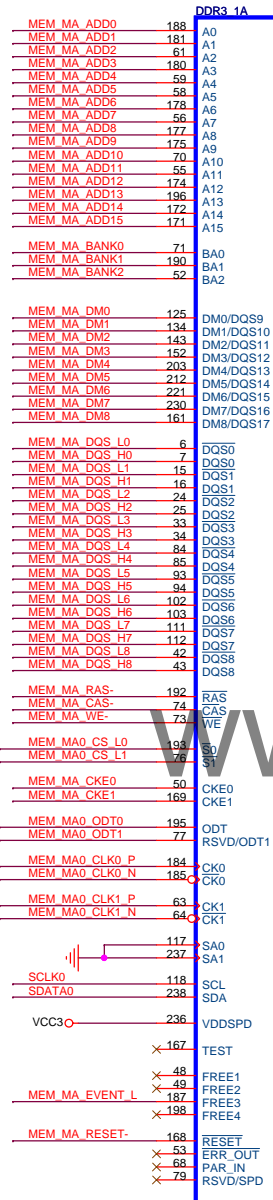


Bottom Side Decoupling

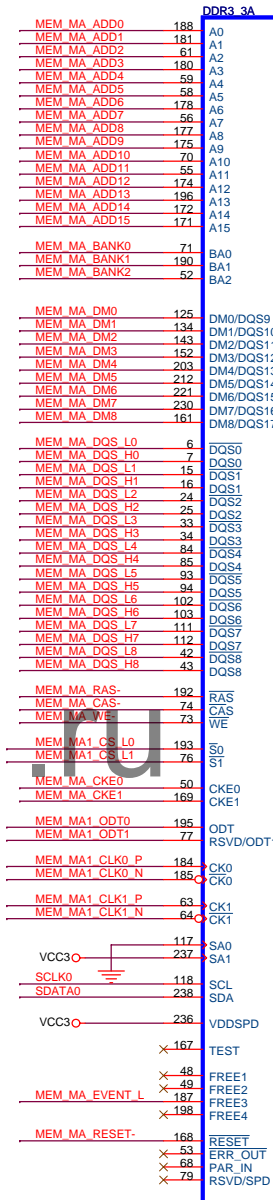
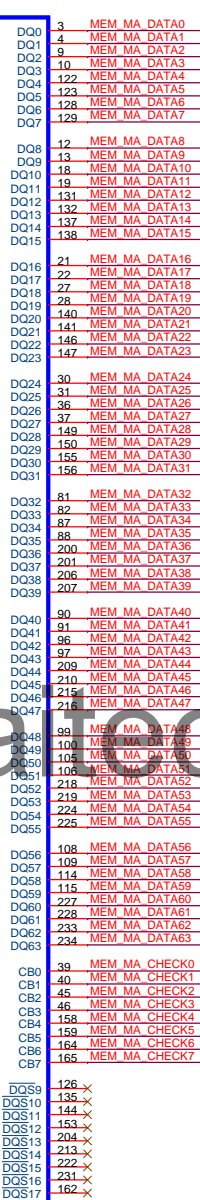




SMBus 0	
Device	8-bit Address (hex)
DIMMA0	A0
DIMMB0	A2
DIMMA1	A4
DIMMB1	A6



DDR3-240P-OR

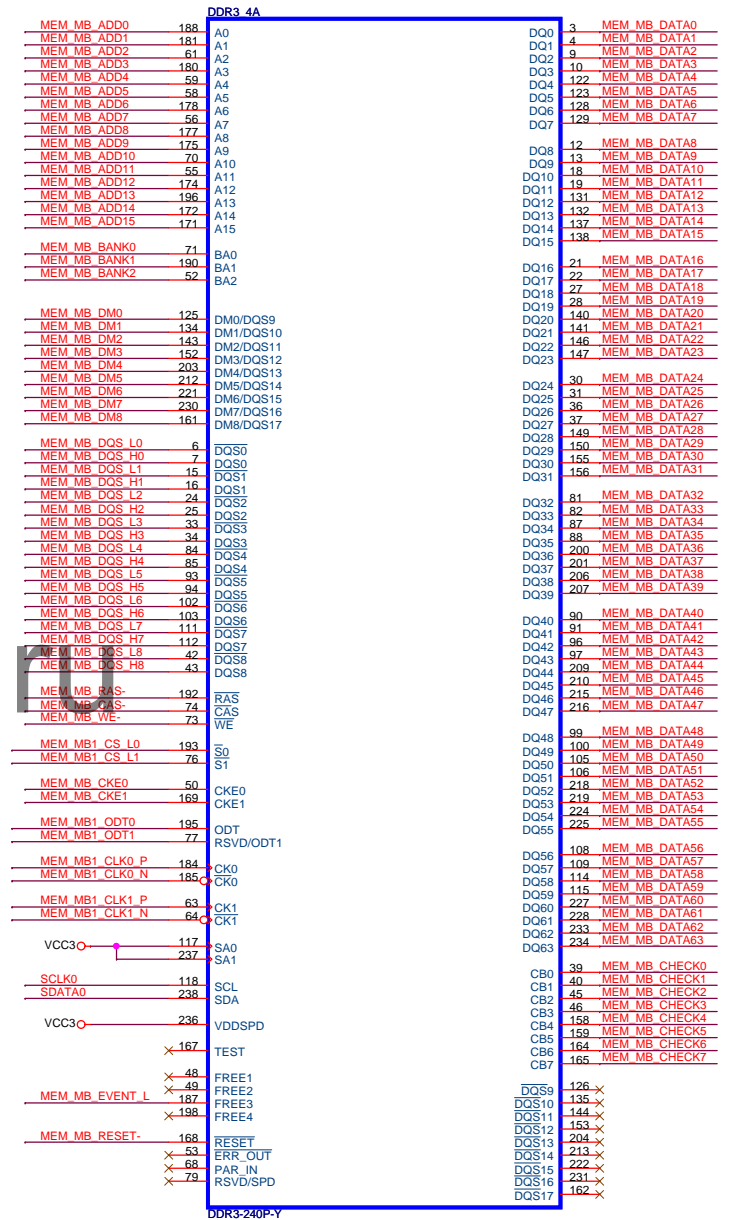
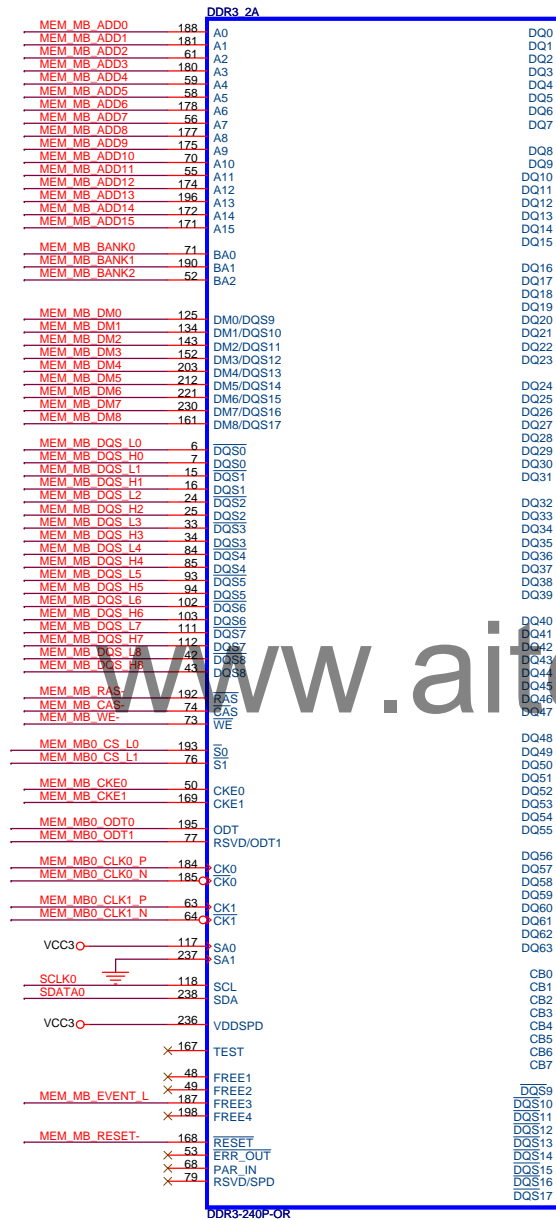
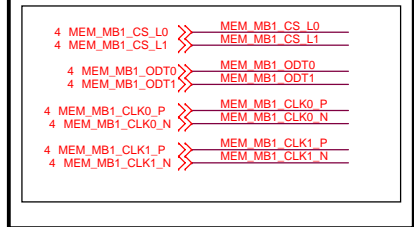
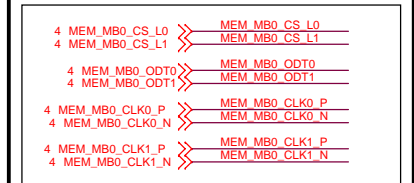
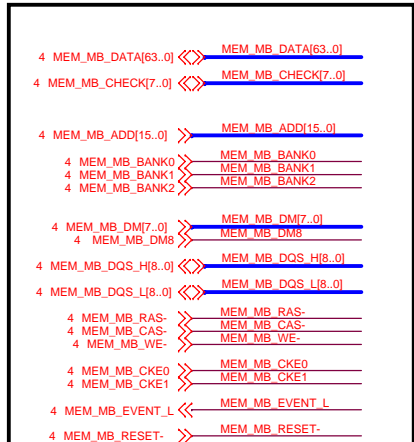
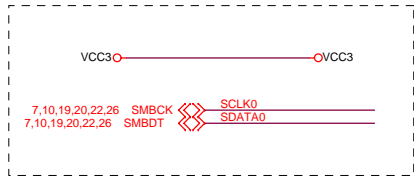


DDR3-240P-Y

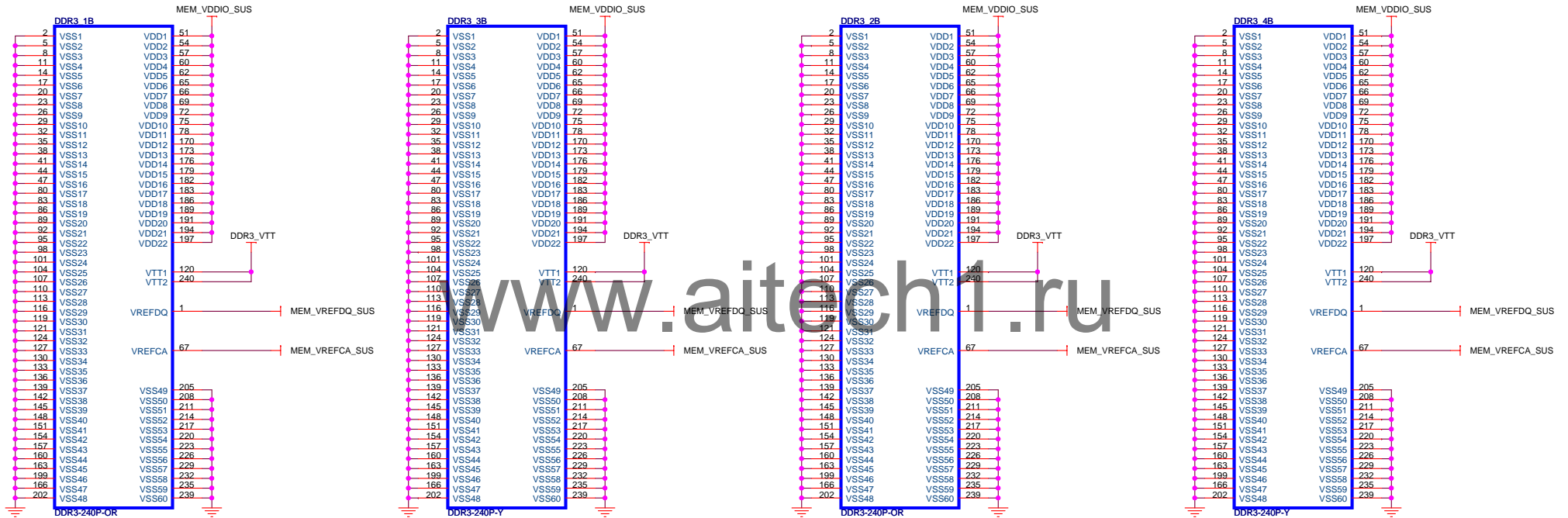
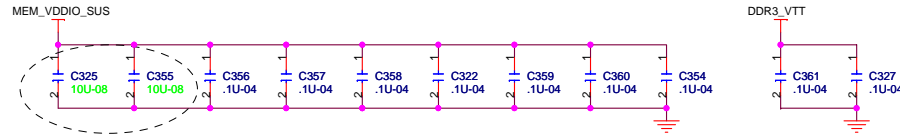
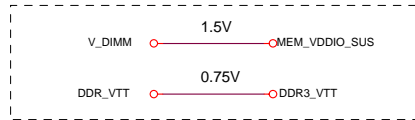


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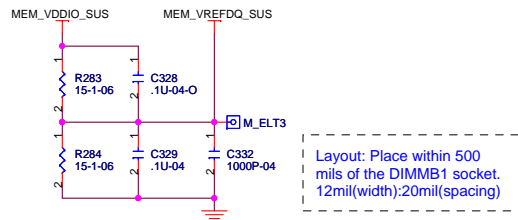
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DDR3 DIMM A CH		
Size	Document Number	Rev
Custom	IC780M-A2	1.0A
Date:	Thursday, October 15, 2009	Sheet 7 of 36



DE-COUPLING CAP FOR DIMMS

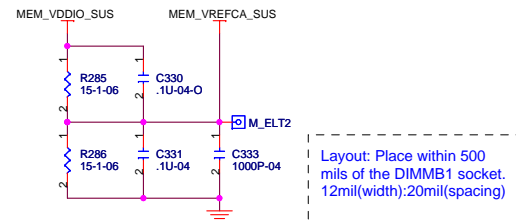


MEM_VREFDQ_SUS



Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width);20mil(spacing)

MEM_VREFCA_SUS

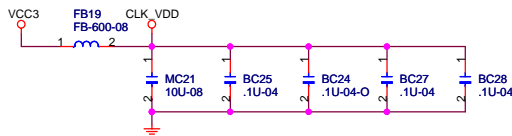


Layout: Place within 500 mils of the DIMMB1 socket.
12mil(width);20mil(spacing)



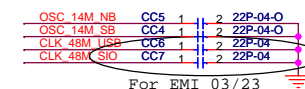
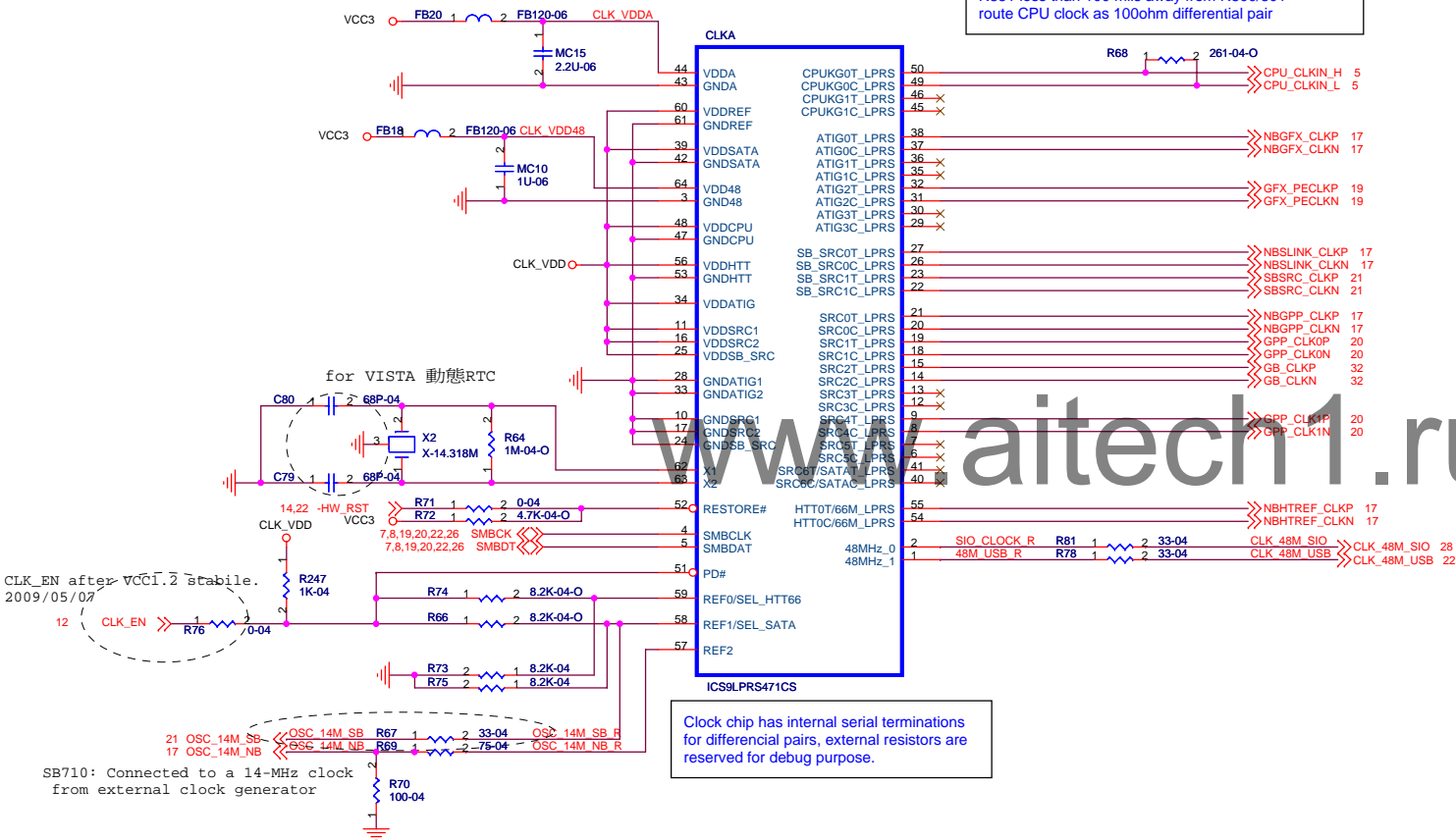
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Title			
DDR3 DIMM PWR			
Size	Document Number	Rev	
Custom	IC780M-A2	1.0A	
Date:	Thursday, October 15, 2009	Sheet	9 of 36



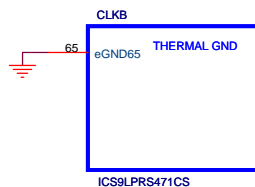
- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO CLK POWER PIN

Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair

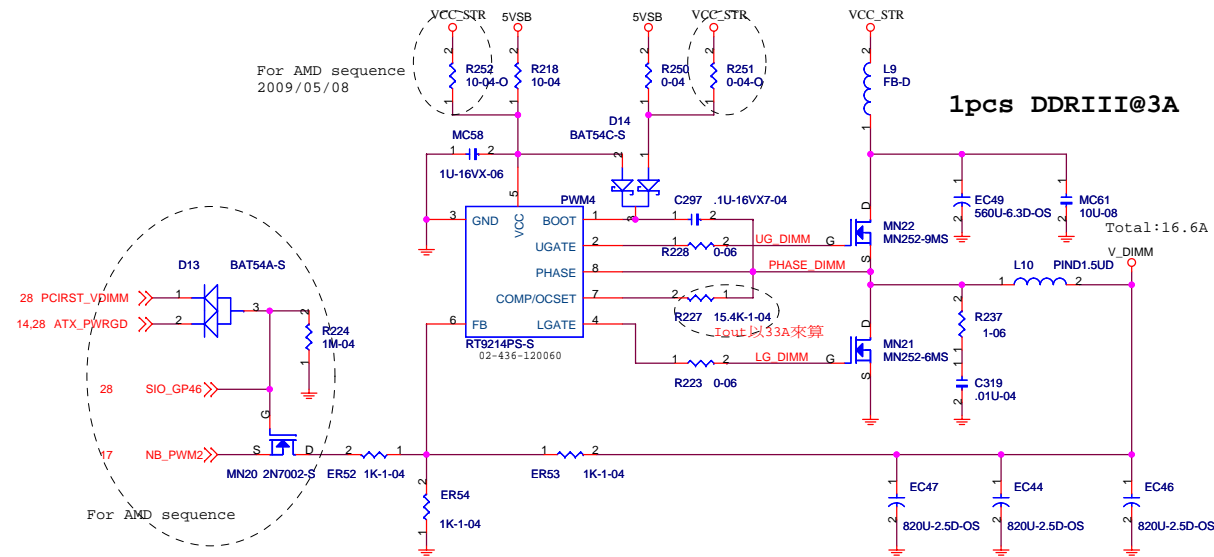


For EMI 03/23

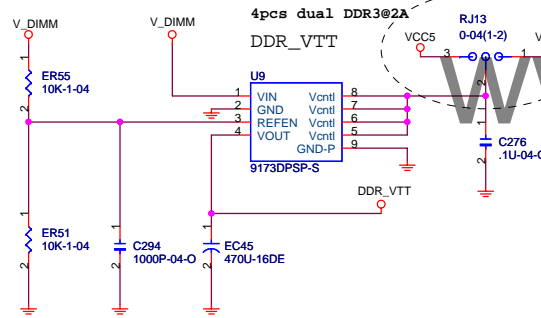
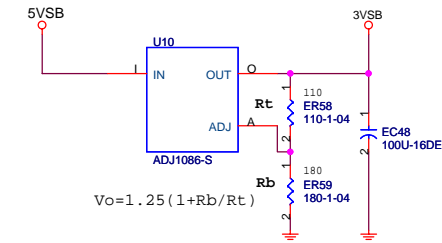
Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



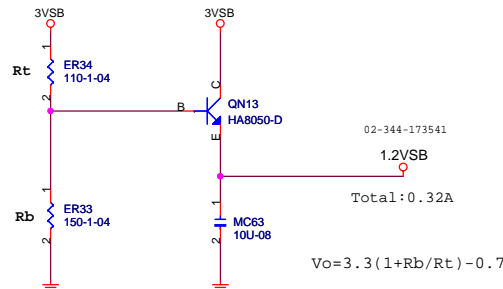
For AMD sequence
2009/05/08



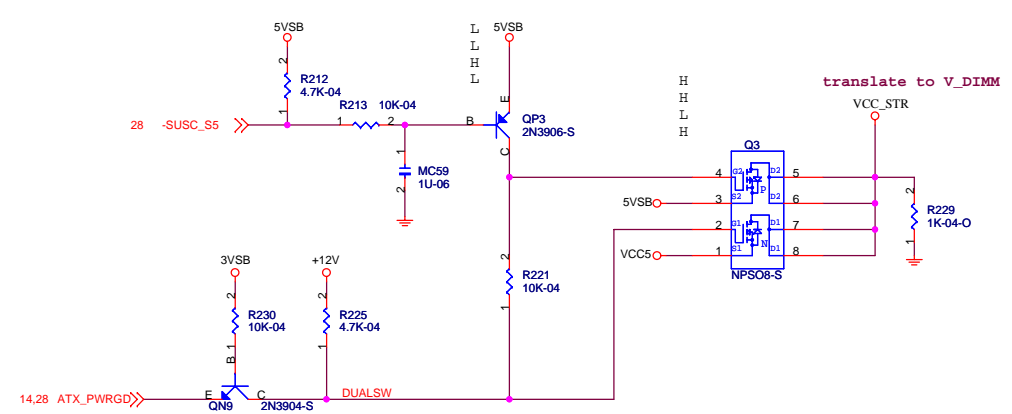
3VSB

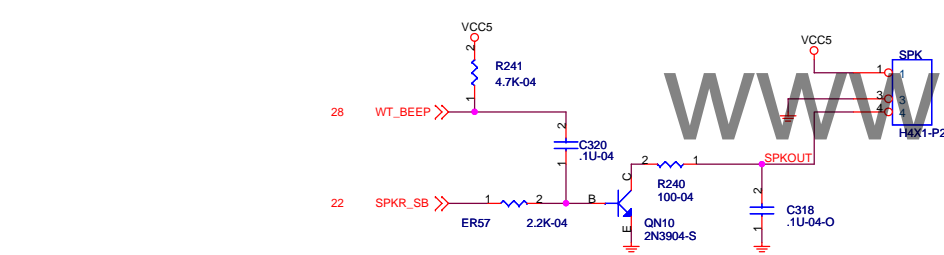
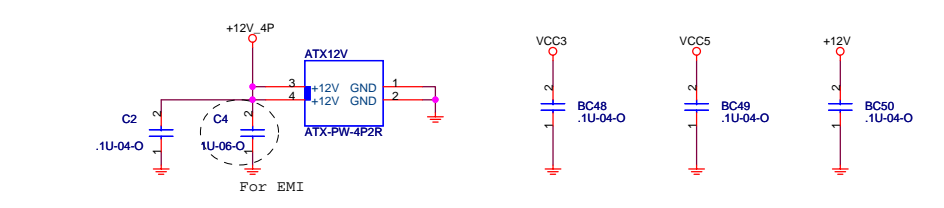
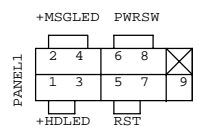
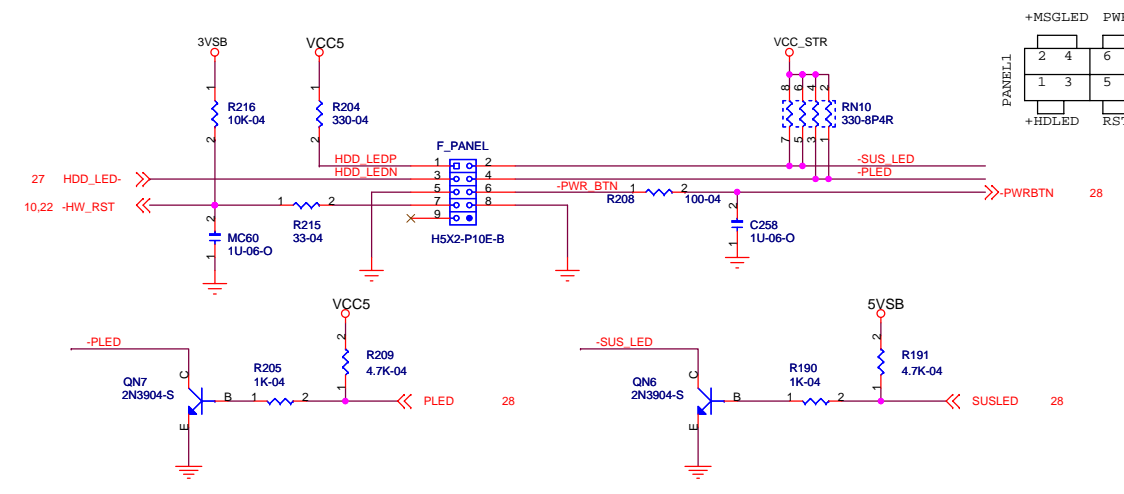
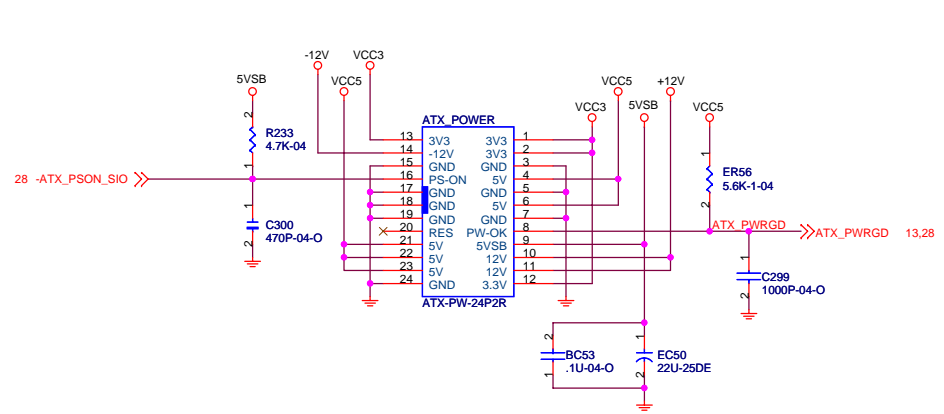


1.2VSB

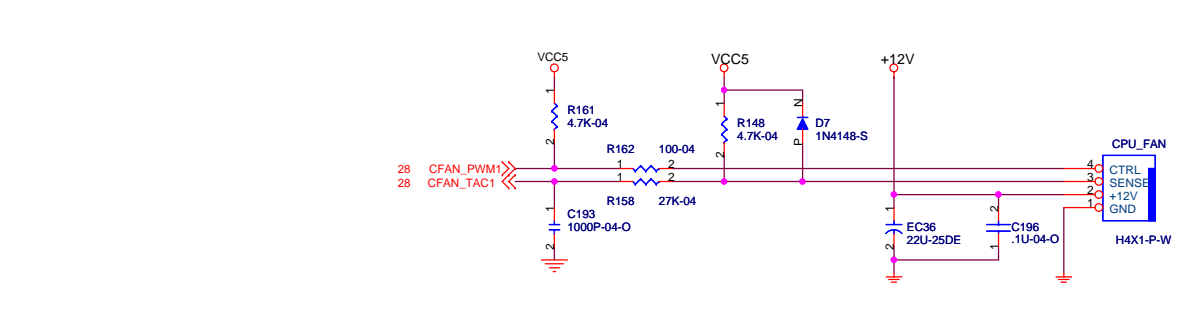
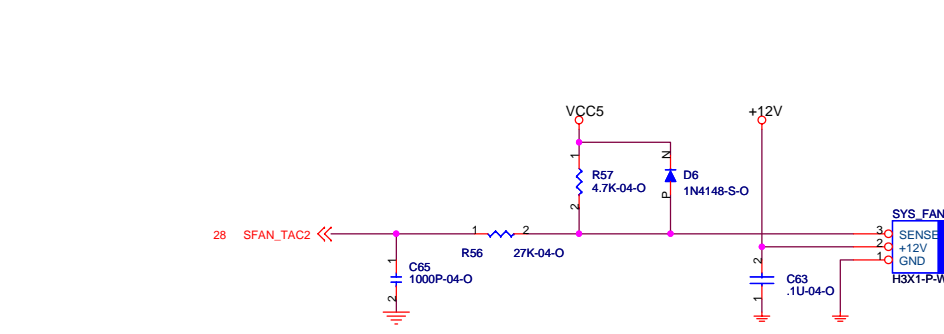


	S5	enter	S0	S0	enter	S3	exit	S3	enter	S5	S5
-SUSC_S5	0	0	1	1	1	0	0	0	0	0	0
ATX_PWRGD	0	1	1	0	1	1	0	0	0	0	0
Q3 pinC	5VSB	5VSB	12V	0	12V	5VSB	5VSB	5VSB	5VSB	5VSB	5VSB
DUALSW	0	12V	12V	0	12V	12V	0	0	0	0	0
VCCSTR	X	VCC5	VCC5	5VSB	VCC5	VCC5	0	0	0	0	0
VDIMM	X	V	V	V	V	V	V	V	V	V	X





	AC_ON	S0	S1	S3	S5
SUSLED (GP41)	0	0	B	B	0
PLED (GP31)	0	1	1	0	0
-SUSLED (PIN2)	1	1	B	B	1
-PLED (PIN4)	1	0	0	1	1
LED STATE	OFF	Green	G-blink	Y-blink	OFF



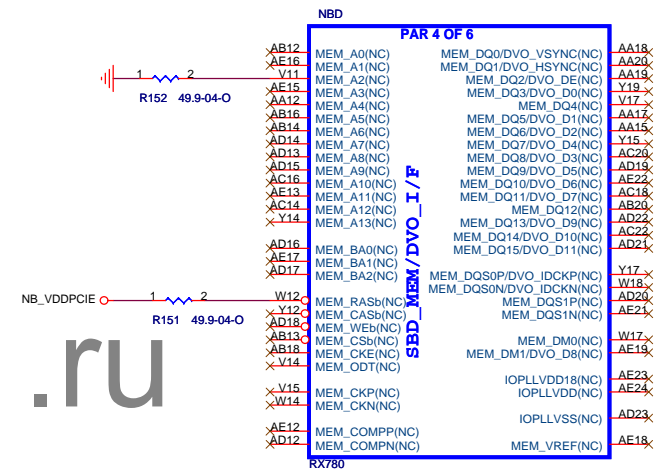
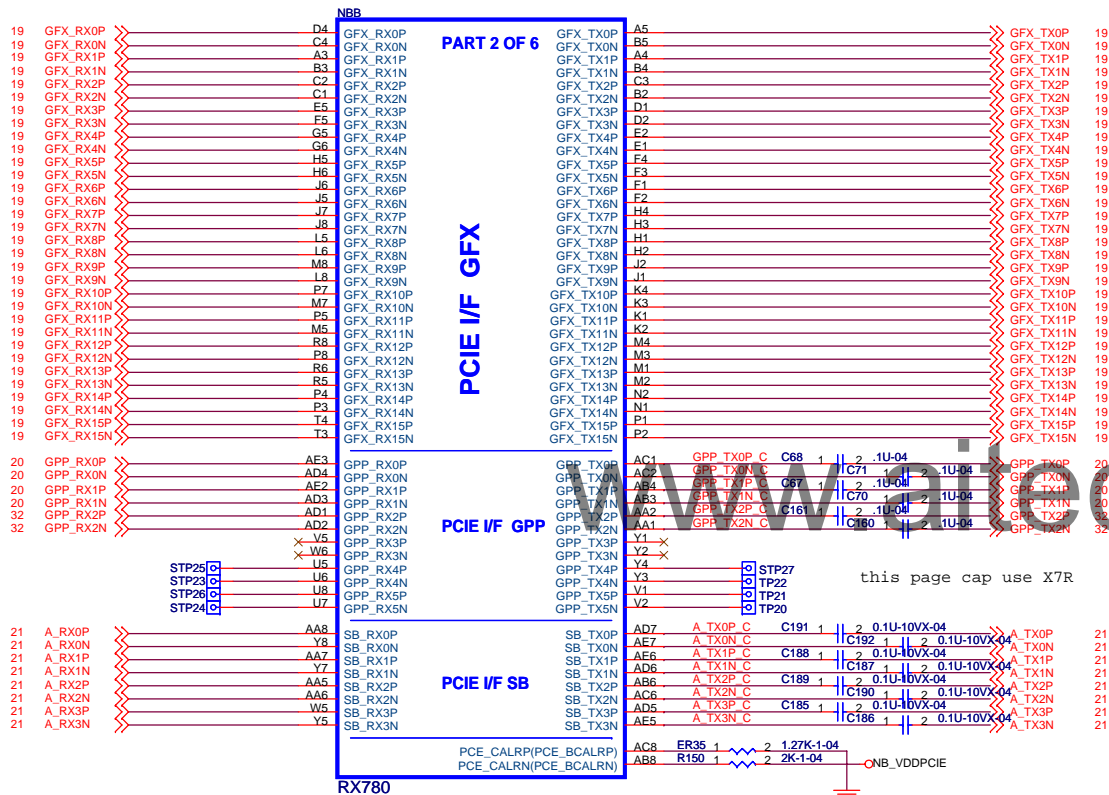
3 HT_CADIN_L[0..15] << HT_CADIN_L[0..15]
3 HT_CADIN_H[0..15] << HT_CADIN_H[0..15]
3 HT_CADOUT_H[0..15] >> HT_CADOUT_H[0..15]
3 HT_CADOUT_L[0..15] >> HT_CADOUT_L[0..15]
3 HT_CLKOUT_H[0..1] >> HT_CLKOUT_H[0..1]
3 HT_CLKOUT_L[0..1] >> HT_CLKOUT_L[0..1]
3 HT_CTLOUT_H[0..1] >> HT_CTLOUT_H[0..1]
3 HT_CTLOUT_L[0..1] >> HT_CTLOUT_L[0..1]
3 HT_CLKIN_H[0..1] << HT_CLKIN_H[0..1]
3 HT_CLKIN_L[0..1] << HT_CLKIN_L[0..1]
3 HT_CTLIN_H[0..1] << HT_CTLIN_H[0..1]
3 HT_CTLIN_L[0..1] << HT_CTLIN_L[0..1]

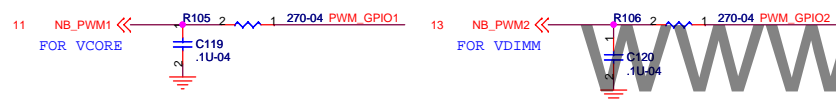
HT_CADOUT_H0 Y25
HT_CADOUT_L0 Y24
HT_CADOUT_H1 V22
HT_CADOUT_L1 V23
HT_CADOUT_H2 V25
HT_CADOUT_L2 V24
HT_CADOUT_H3 U24
HT_CADOUT_L3 U25
HT_CADOUT_H4 T25
HT_CADOUT_L4 T24
HT_CADOUT_H5 P22
HT_CADOUT_L5 P23
HT_CADOUT_H6 P23
HT_CADOUT_L6 P24
HT_CADOUT_H7 N24
HT_CADOUT_L7 N25
HT_CADOUT_H8 AC24
HT_CADOUT_L8 AC25
HT_CADOUT_H9 AB25
HT_CADOUT_L9 AB24
HT_CADOUT_H10 AA24
HT_CADOUT_L10 AA25
HT_CADOUT_H11 Y22
HT_CADOUT_L11 Y23
HT_CADOUT_H12 W21
HT_CADOUT_L12 W20
HT_CADOUT_H13 V21
HT_CADOUT_L13 U20
HT_CADOUT_H14 U21
HT_CADOUT_L14 U19
HT_CADOUT_H15 U18
HT_CLKOUT_H0 T22
HT_CLKOUT_L0 T23
HT_CLKOUT_H1 AB23
HT_CLKOUT_L1 AA22
HT_CTLOUT_H0 M22
HT_CTLOUT_L0 M23
HT_CTLOUT_H1 R21
HT_CTLOUT_L1 R20
HT_RXCALP C23
HT_RXCALN A24
HT_RXCAD0P
HT_RXCAD0N
HT_RXCAD1P
HT_RXCAD1N
HT_RXCAD2P
HT_RXCAD2N
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HT_TXCAD7N
HT_TXCAD8P
HT_TXCAD8N
HT_TXCAD9P
HT_TXCAD9N
HT_TXCAD10P
HT_TXCAD10N
HT_TXCAD11P
HT_TXCAD11N
HT_TXCAD12P
HT_TXCAD12N
HT_TXCAD13P
HT_TXCAD13N
HT_TXCAD14P
HT_TXCAD14N
HT_TXCAD15P
HT_TXCAD15N
HT_TXCLK0P
HT_TXCLK0N
HT_TXCLK1P
HT_TXCLK1N
HT_TXCTL0P
HT_TXCTL0N
HT_TXCTL1P
HT_TXCTL1N
HT_TXCALP
HT_TXCALN

PART 1 OF 6

HYPER TRANSPORT CPU I/F

D24
D25
E24
E25
F24
F25
F22
H23
H22
J25
J24
K25
K23
K22
F21
G21
G20
H21
J20
J21
J18
J19
M19
L18
M21
P21
P18
M18
J24
J25
L21
L20
M24
M25
P21
R18
B24
B25
HT_CADIN_H0
HT_CADIN_L0
HT_CADIN_H1
HT_CADIN_L1
HT_CADIN_H2
HT_CADIN_L2
HT_CADIN_H3
HT_CADIN_L3
HT_CADIN_H4
HT_CADIN_L4
HT_CADIN_H5
HT_CADIN_L5
HT_CADIN_H6
HT_CADIN_L6
HT_CADIN_H7
HT_CADIN_L7
HT_CADIN_H8
HT_CADIN_L8
HT_CADIN_H9
HT_CADIN_L9
HT_CADIN_H10
HT_CADIN_L10
HT_CADIN_H11
HT_CADIN_L11
HT_CADIN_H12
HT_CADIN_L12
HT_CADIN_H13
HT_CADIN_L13
HT_CADIN_H14
HT_CADIN_L14
HT_CADIN_H15
HT_CADIN_L15
HT_CLKIN_H0
HT_CLKIN_L0
HT_CLKIN_H1
HT_CLKIN_L1
HT_CTLIN_H0
HT_CTLIN_L0
HT_CTLIN_H1
HT_CTLIN_L1
HT_TXBCLP
HT_TXBCLN
HT_TXCALP
HT_TXCALN



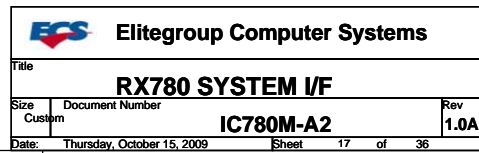


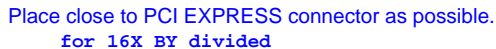
```
Enables the Test Debug Bus using GPIO.
1 : Disable ( Can still be enabled using
nbcfg register access)
0 : Enable
```

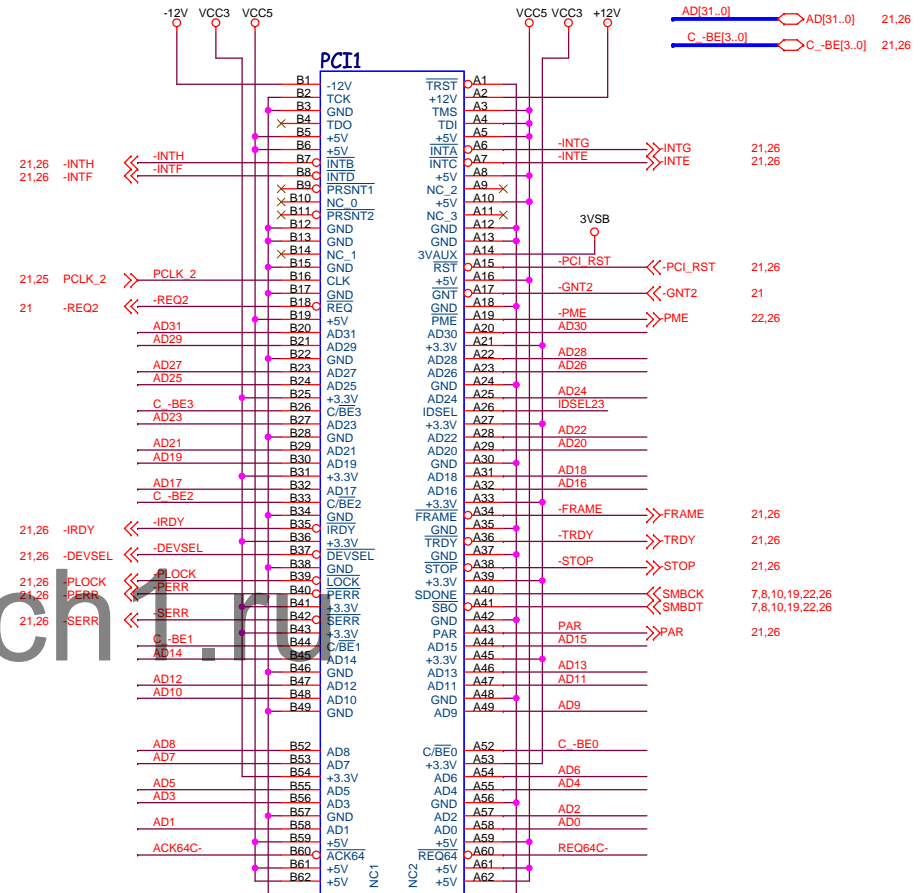
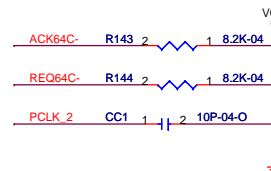
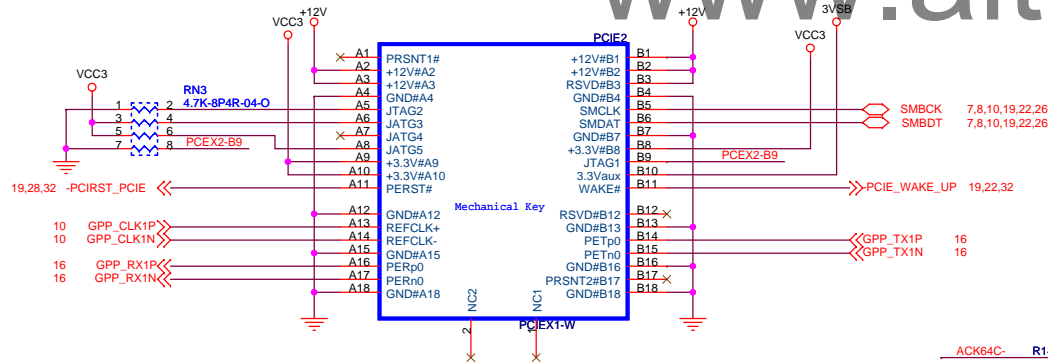
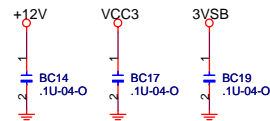
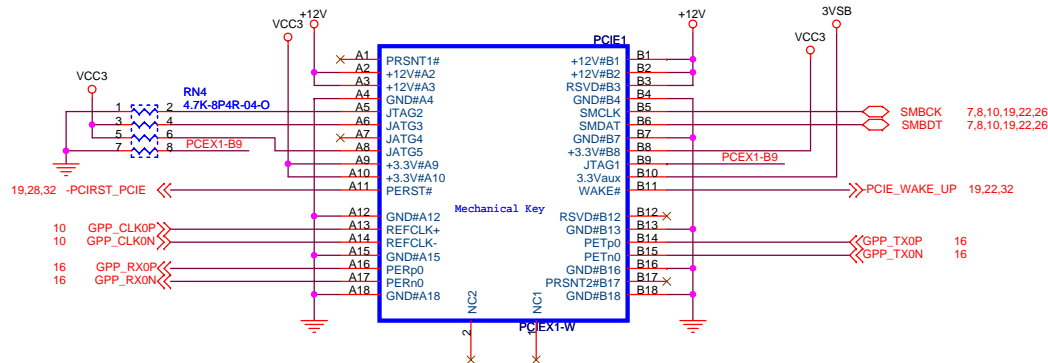
```
These pin straps are used to configure PCI-E GPP mode.
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011
```

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
```

```
Enables the Test Debug Bus using PCIE bus
1 : Disable ( Can still be enabled using nbcfg register access )
0 : Enable
```

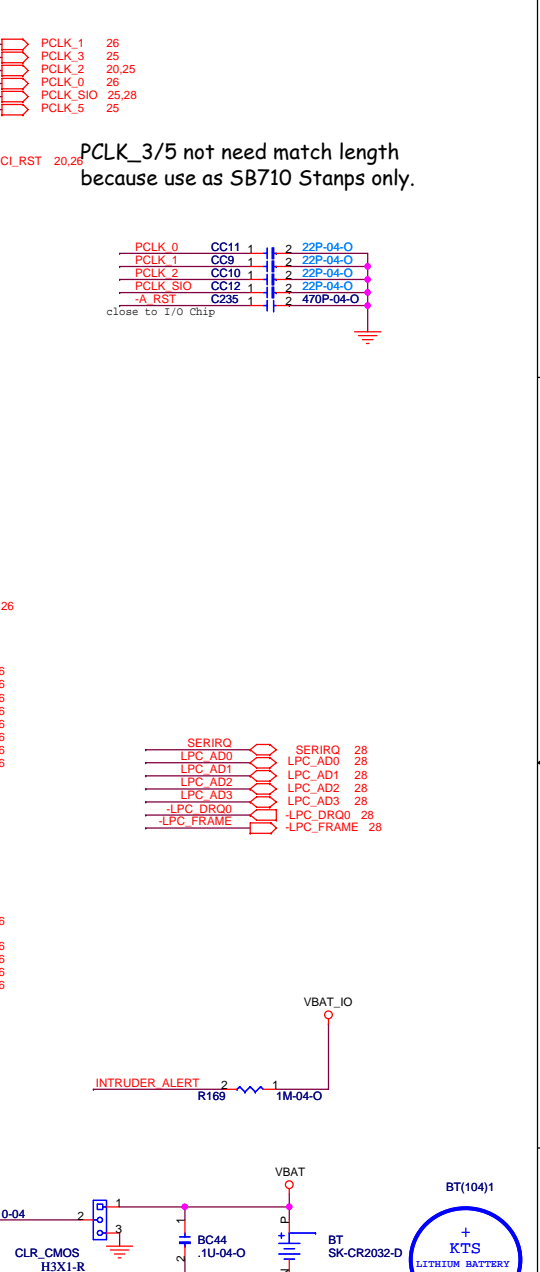
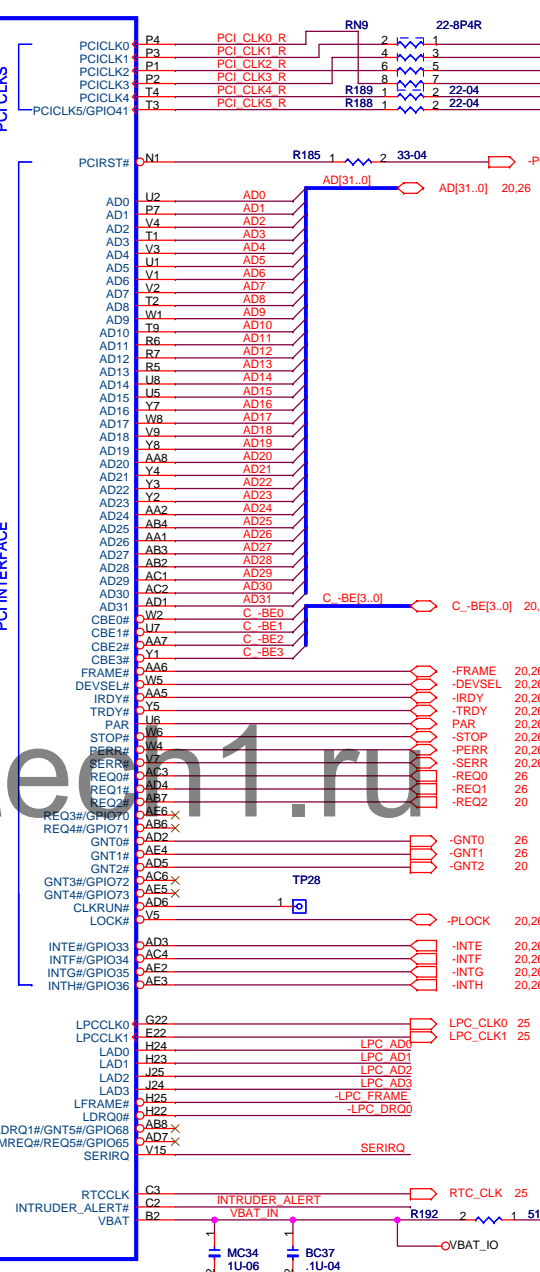
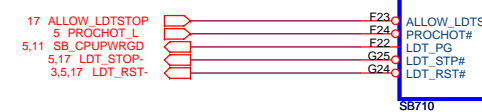
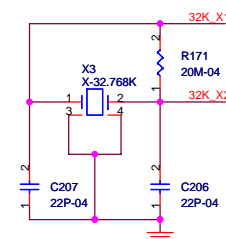
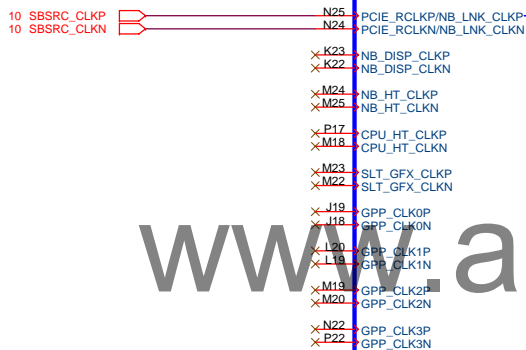
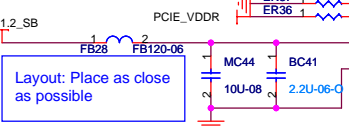
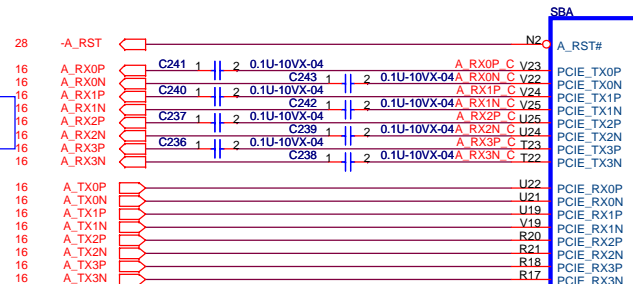






REQ2;GNT2
IDSEL:23
GHEF

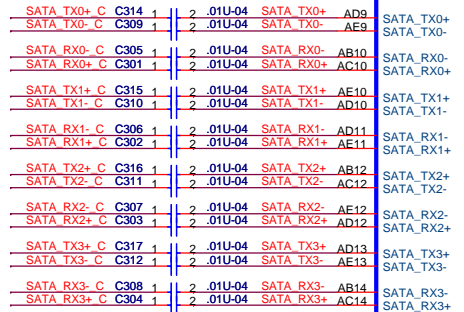
PLACE THESE PCIE AC COUPLING CAPS CLOSE TO BGA



POWER EXPRESS SUPPORT

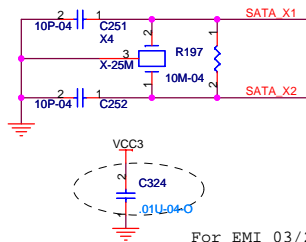
PE_GPIO0 MXM RESET H: Enable
 PE_GPIO1 MXM POWER ENABLE H: Enable
 PE_GPIO2 MODE SWITCH H:MXM L:NB
 TMDS_HPD0 MXM HOT PLUG

PLACE SATA AC COUPLING
CAPS CLOSE TO SB710

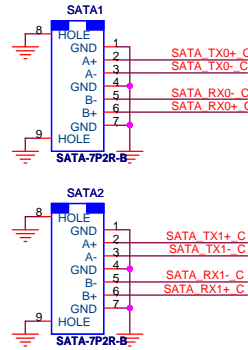
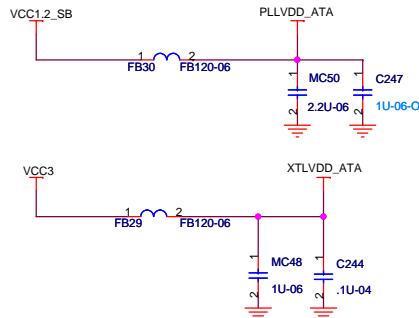


PLACE SATA_CAL RES
VERY CLOSE TO BALL OF
SB700/SB710

NOTE:
SR3 IS 1K 1% FOR 25MHz
XTAL 4.99K 1% FOR 100MHz
INTERNAL CLOCK



For EMI 03/23



SERIAL ATA

SATA PWR

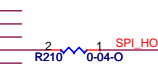
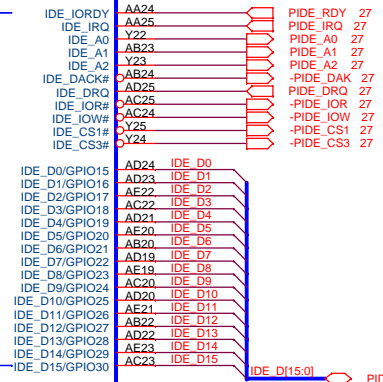
HW MONITOR

SB710
Part 2 of 5

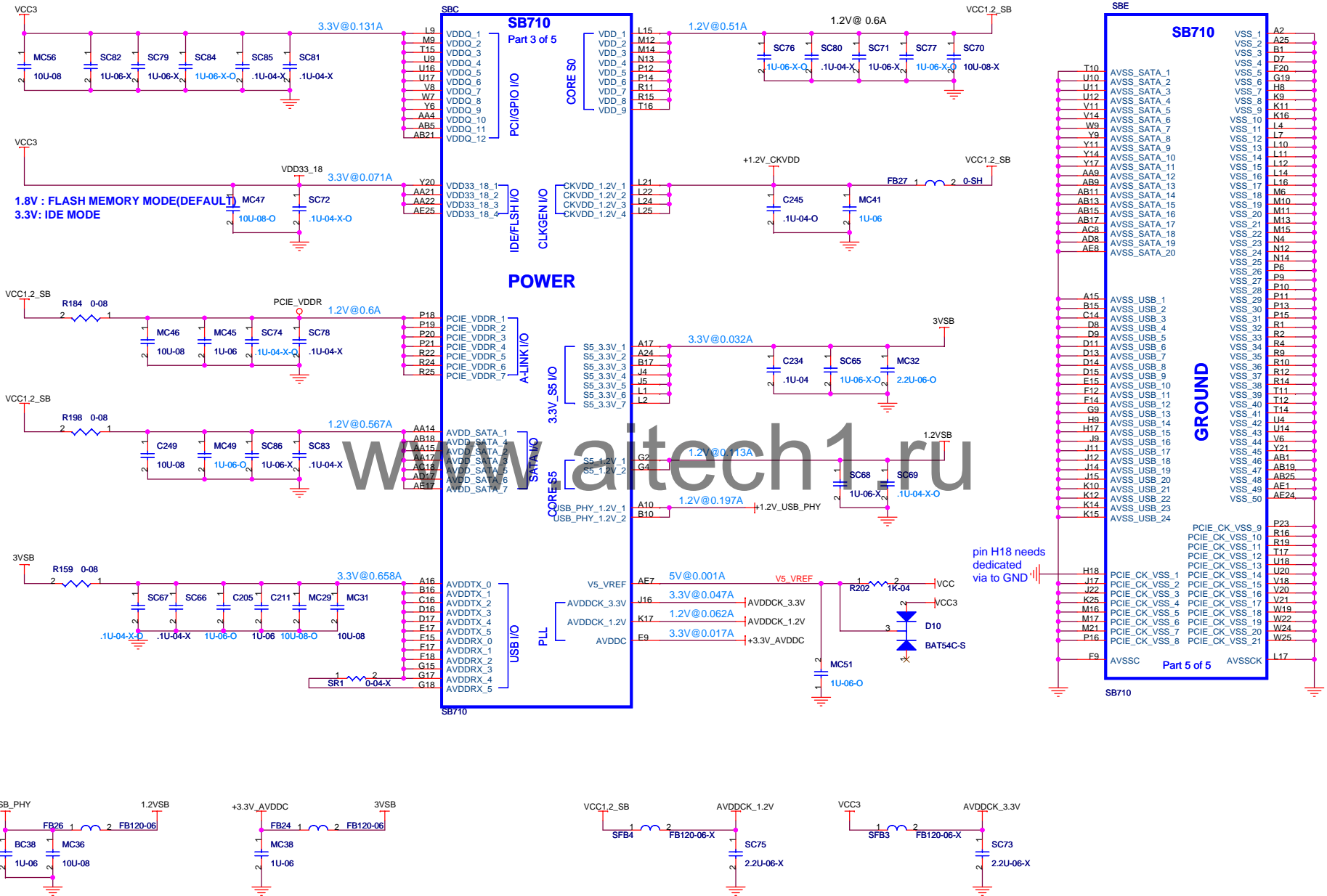
ATA 66/100/133

SPI ROM

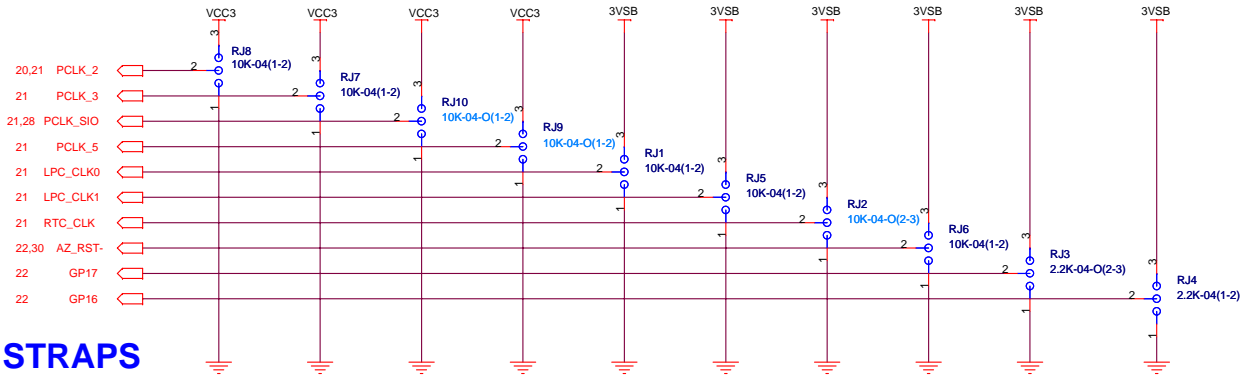
HW MONITOR



PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.



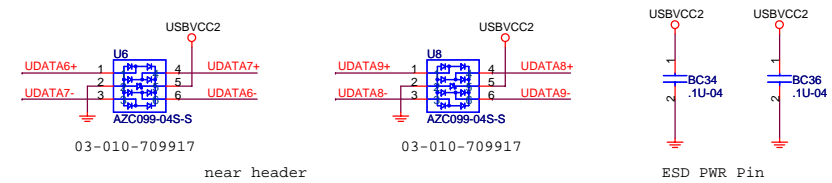
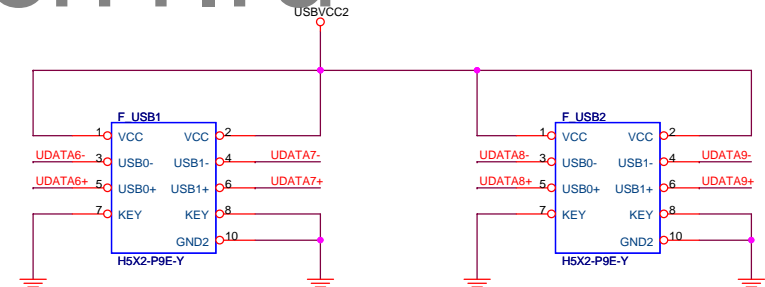
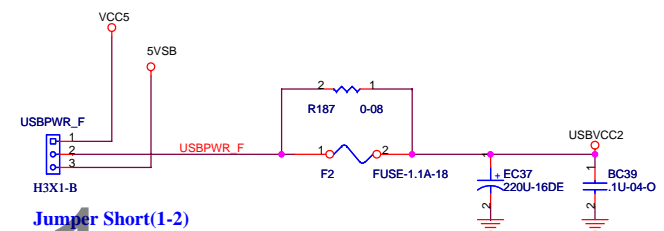
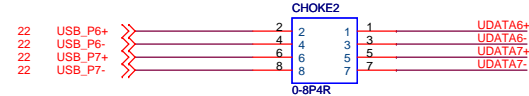
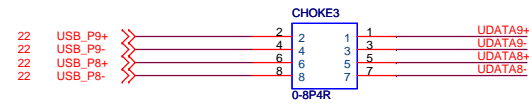
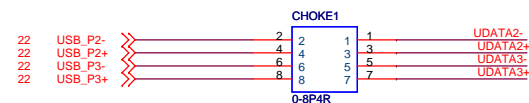
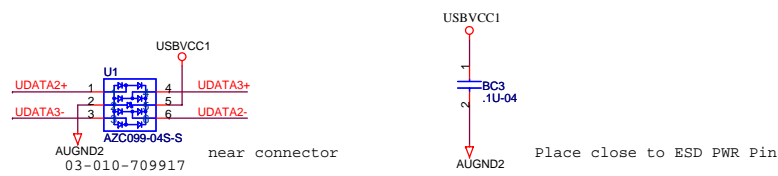
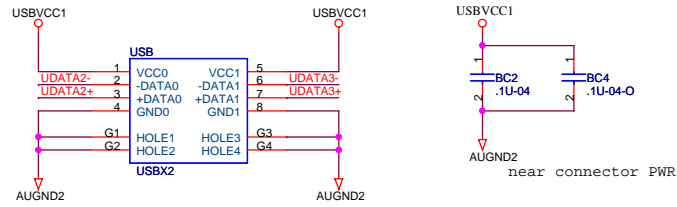
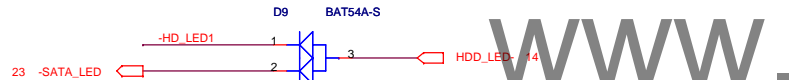
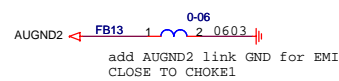
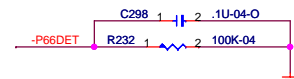
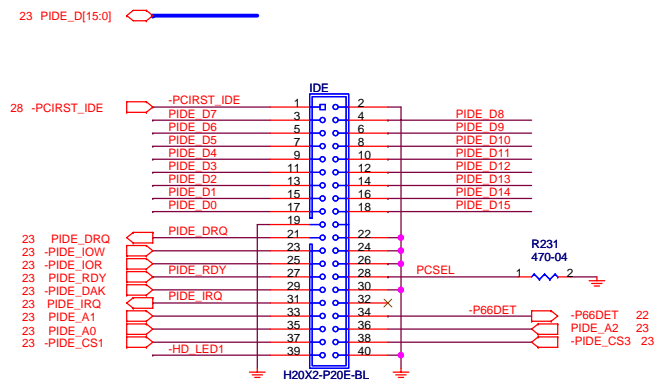
NOTE: SB710 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

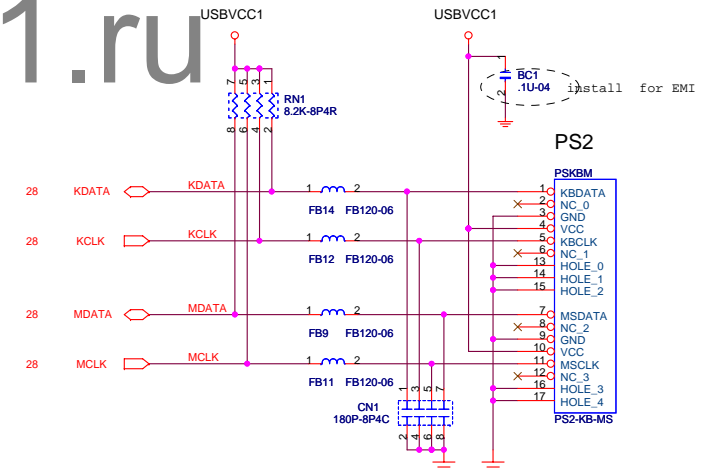
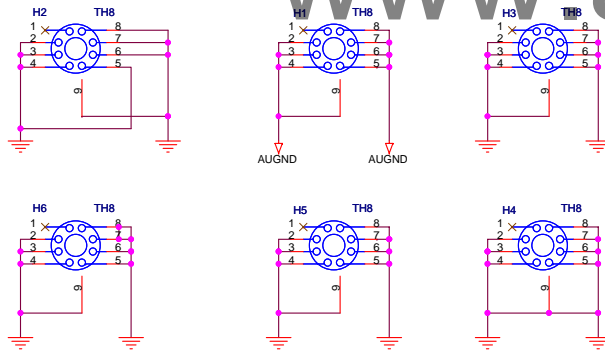
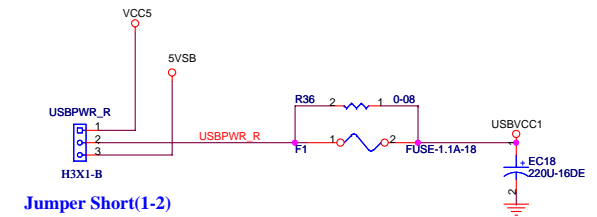
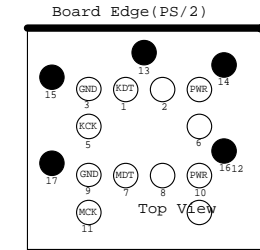
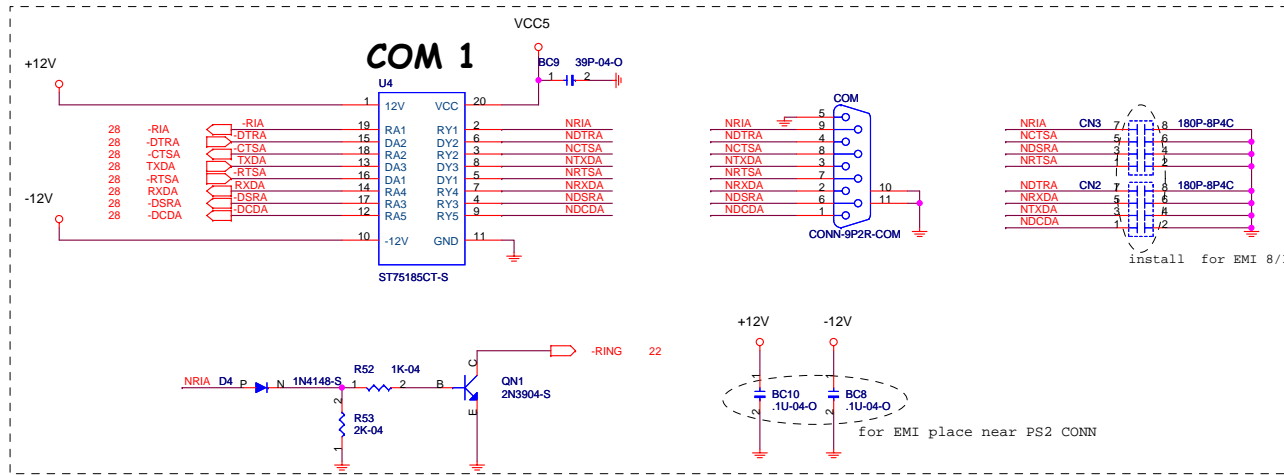


REQUIRED STRAPS

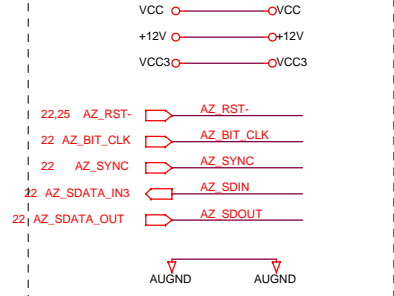
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17	GP16
PULL HIGH	Watchdog ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	IMC Enable	CLKGEN ENABLED	INTERNAL RTC	PCI ROM BOOT Enable	ROM TYPE: H, H = Reserved H, L = SPI ROM	
PULL LOW	Watchdog DISABLED	IGNORE DEBUG STRAPS			IMC Disable	CLKGEN DISABLED	EKT. RTC (PD on X1, apply 32KHz to RTC_CLK)	PCI ROM BOOT Disable	L, H = LPC ROM	L, L = FW ROM

A14
SPI ROM:
IMC_GPO17-->SB710/SB750 A14 Not connected.

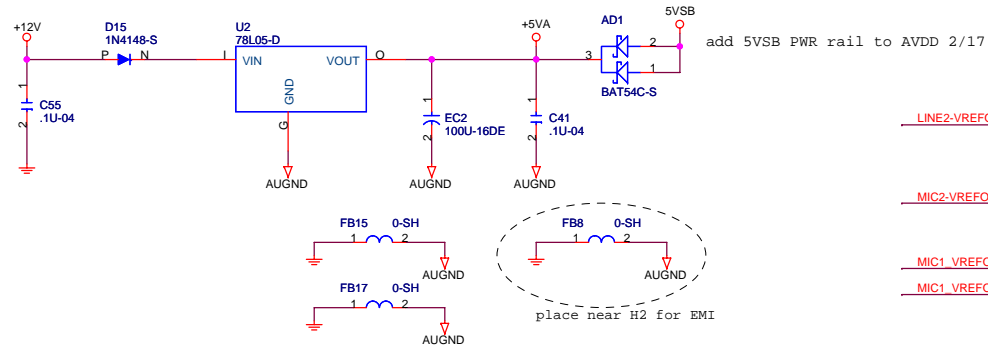




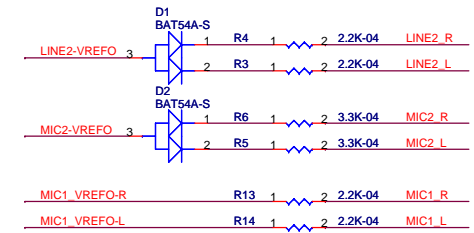
External Connection



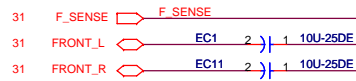
When you found some bug, please inform Ren(ext:665) to update circuit.



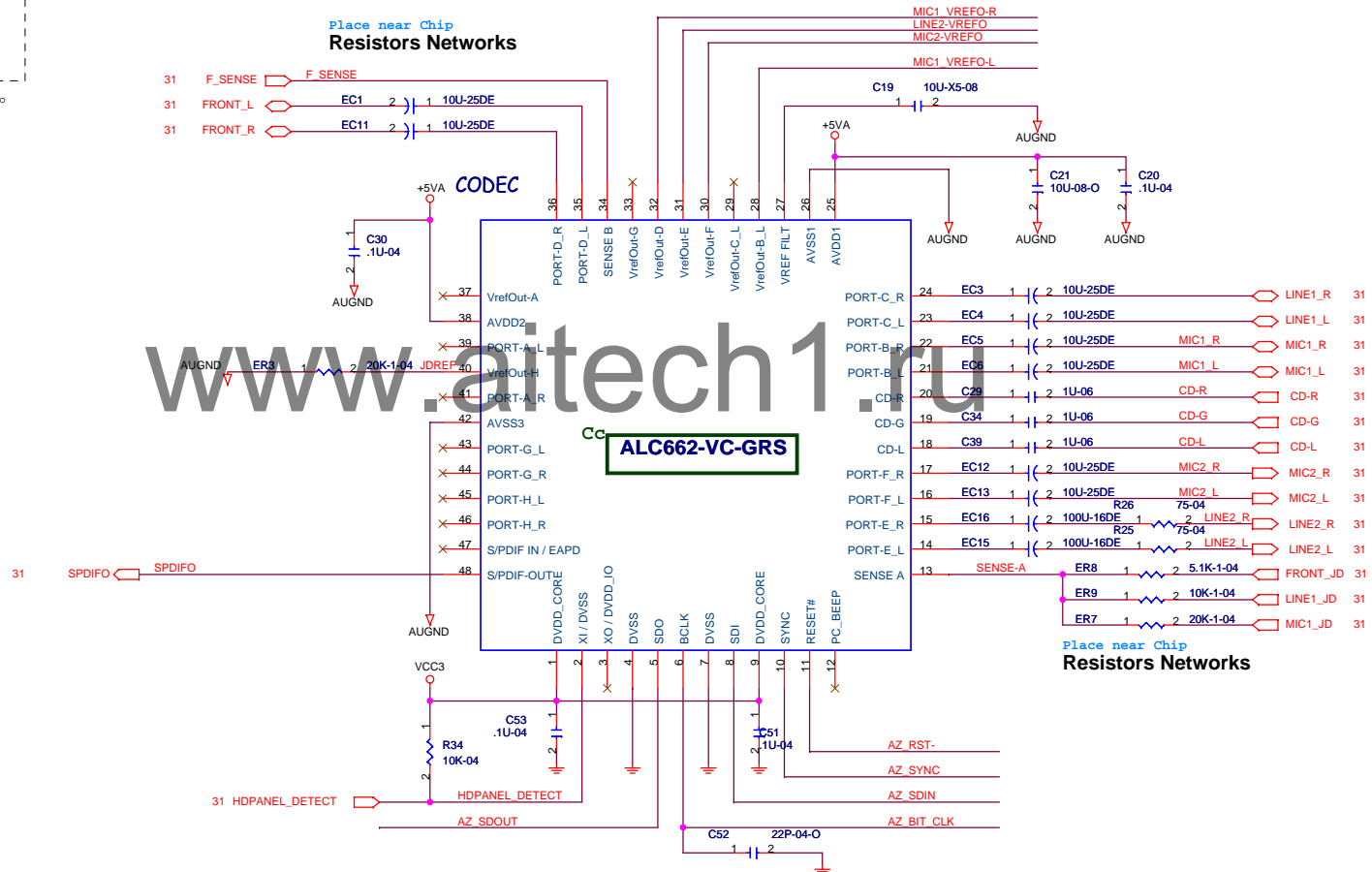
MIC Bias



Place near Chip Resistors Networks

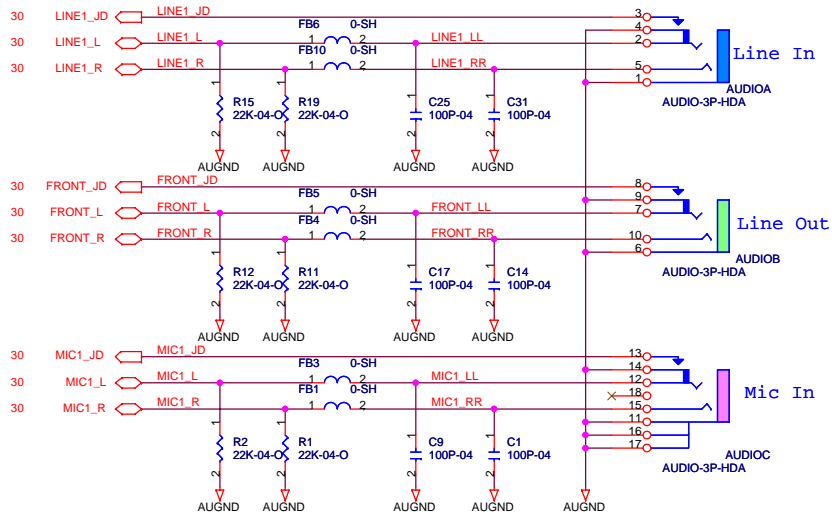


CODEC

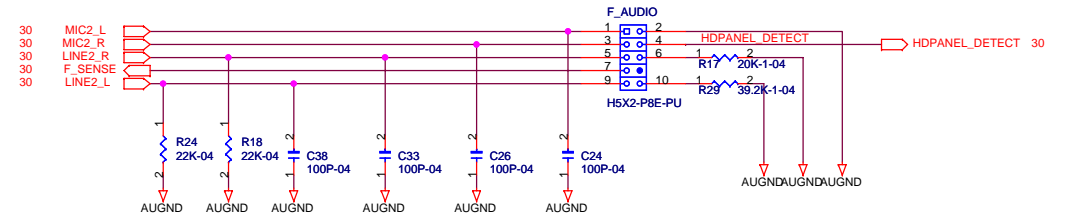


Place near Chip Resistors Networks

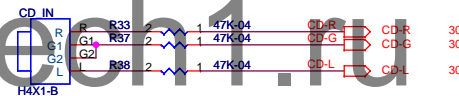
REAR-AUDIO



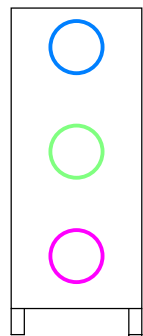
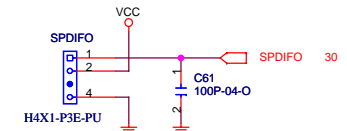
FRONT-AUDIO



CD_IN



SPDIF-OUT



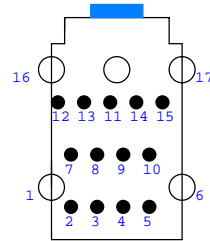
FRONT VIEW

Line in

Front out

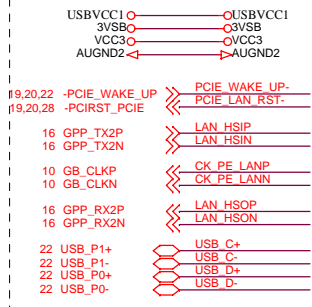
Mic in

TOP VIEW



TOP VIEW

External Connection



When you found some bug, please inform Ren(ext:665) to update circuit.

新手提醒:

- LAN_HSOP/N請接到SB的PCIE RX端
- LAN_HSIP/N請接到SB的PCIE TX端
- LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap

RTL8103EL-GR
01-278-103350

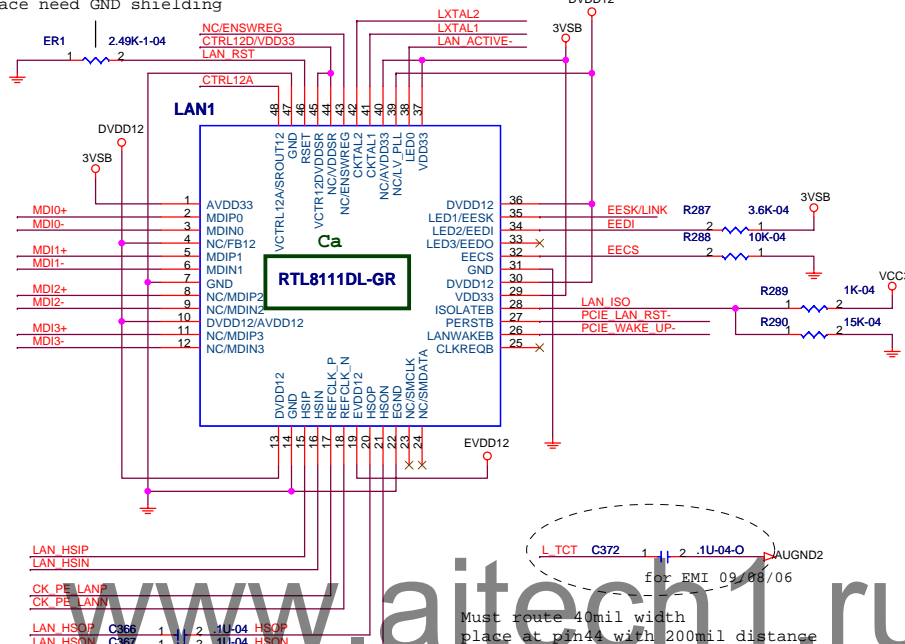
BOM Difference

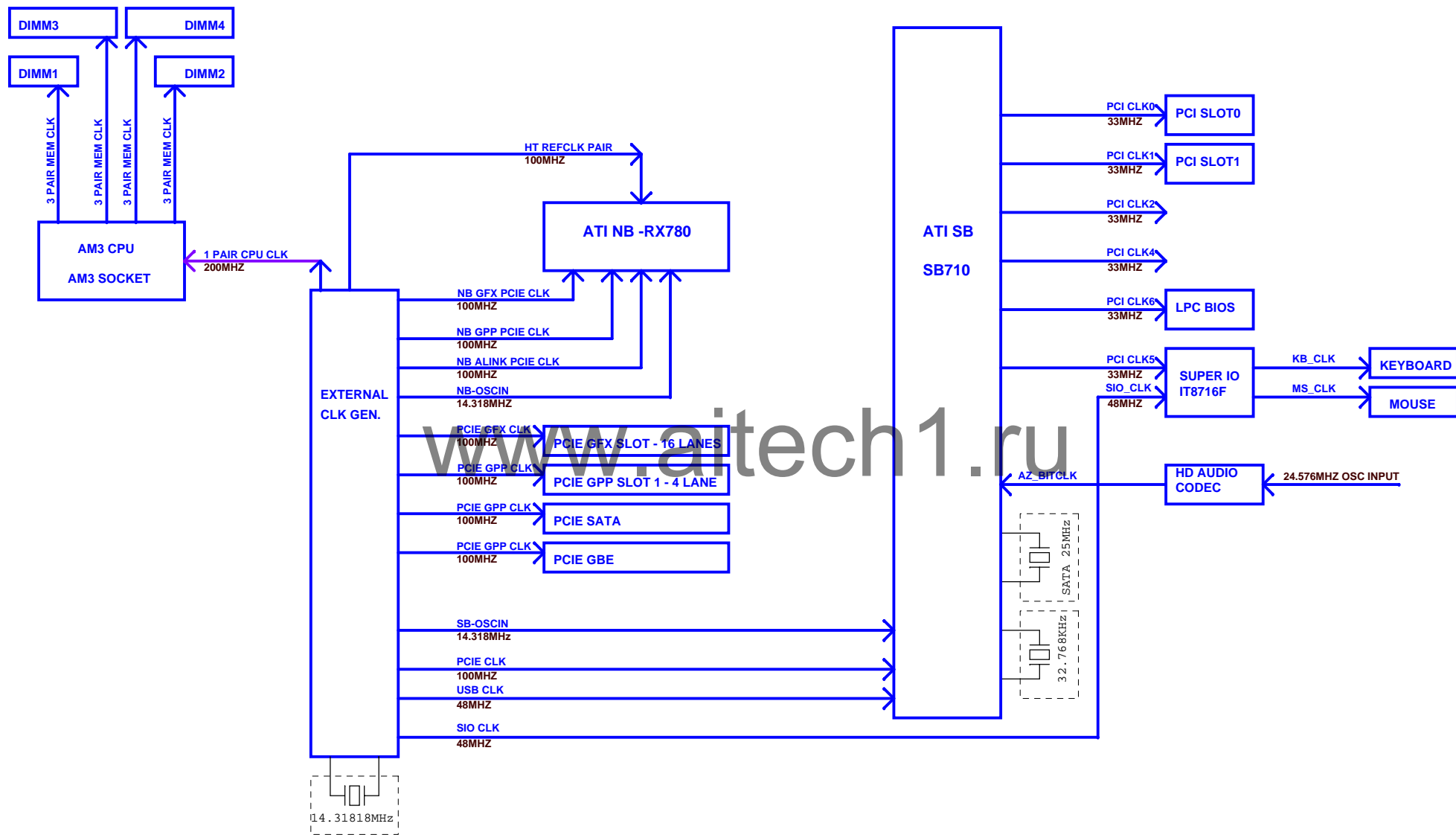
	RTL8111DL-GR 1000M	RTL8103EL-GR 10/100M
Ca	RTL8111DL-GR	RTL8103EL-GR
Cb	X	V
Cc	0-04	.01U-04
Cd	X	V
Ce	V	X
Cf	USBX2-LAN-1000	USBX2-LAN-100

Power Difference

	RTL8111D	RTL8103E
AVDD33 VDD33	3.3V 3VSB供應	3.3V 3VSB供應
CTRL12A	Switching Output	1.2V pinself 供應
DVDD12	1.2V CTRL12A供應	1.2V pinself 供應
EVDD12	1.2V CTRL12A供應	1.2V pinself 供應

RSET電阻需close to LAN
Trace need GND shielding





SB700 PinC26 GPIO8:PCEI_GFX1_PRSNT-
SB700 PinD26 GPIO9:-P66DET

8726 GPIO使用:
Pin14-GPIO34用作WT_BEEP
Pin13-GPIO35 用作NB_PWM_enable控制
Pin18-GPIO31 PLED
Pin78-GP41 SUSLED
Pin28-GP17 -WP_ROM
Pin79-GPIO40: SIO_VDUAL control 5vdual
Pin28-GP22-THRM
Pin27-GP20:-LPC_SMI
Pin70-GP46:Control v_dimm

PCI SLOT1:REQ0;GNT0 IDSEL:21 INT:EFGH
PCI SLOT2:REQ1;GNT1 IDSEL:22 INT:FGHE
PCI SLOT3:REQ2;GNT2 IDSEL:23 INT:GHEF

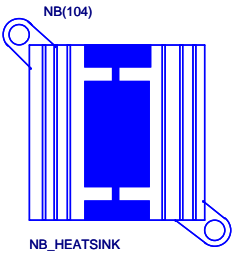
NB_PWM1: Regulate VCC_CORE
NB_PWM2: Regulate V_DIMM

GPP:0-->PCIEx1
GPP:2-->GIGA LAN

For 103



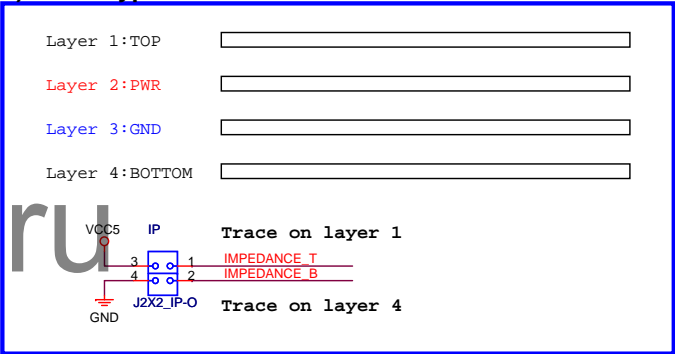
For 104



PCB Impedance control

Impedance (ohm)	Trace Width (mil) (S/W/S)	Trace Length (inch)	Pre-preg	
60	5 (20/5/20)	6	2116	V
50	4 (50/4/50)	6	1080	
42	6 (50/6/50)	6	1080	

1)Circuit type 1



Notes:

- 1). "PWR" net means inner power plane under impedance trace.
- 2). "GND" net means inner ground plane under impedance trace.
- 3). IP1 footprint is J2X2_IP
- 4). After netlist running, please specially take care the single net name: "IMPEDANCE_T" and "IMPEDANCE_B".



Elitegroup Computer Systems

Title

ATTENTION

Size
Custom

Document Number

IC780M-A2

Rev

1.0A

Date: Thursday, October 15, 2009

Sheet 34 of 36

